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COMMUNICATING FOR COMMUNICATIONS TEST

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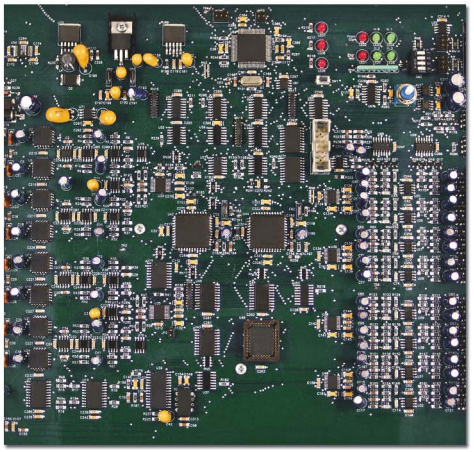
High Fidelity Audio for:

Automotive

Consumer

Professional



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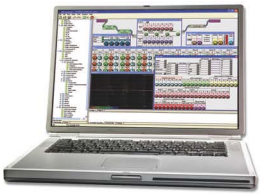

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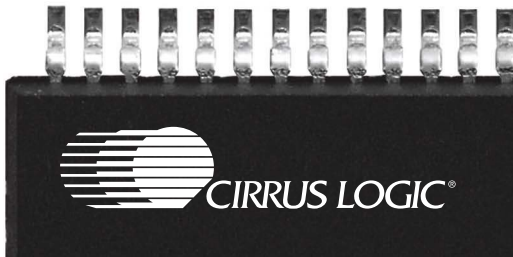

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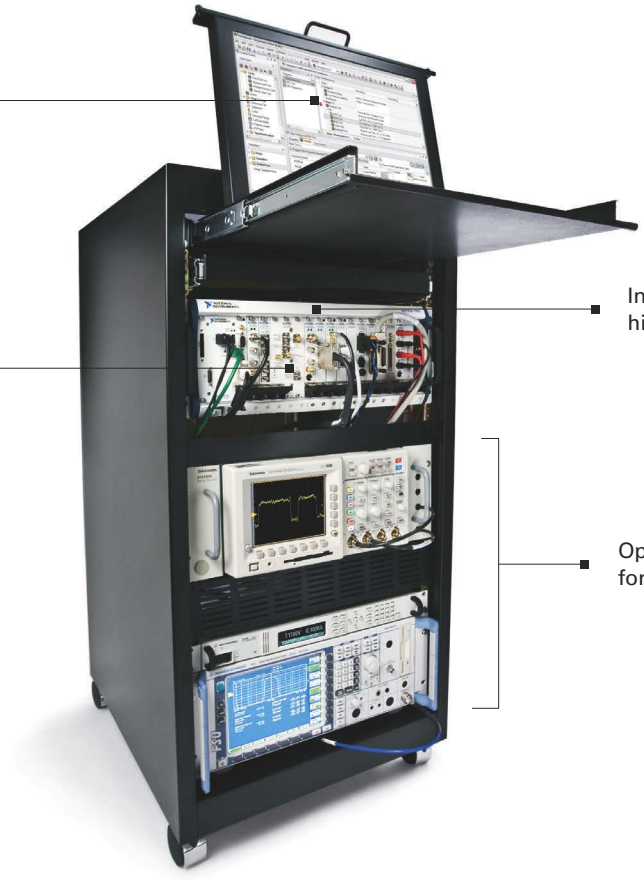

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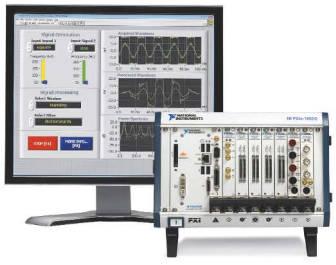

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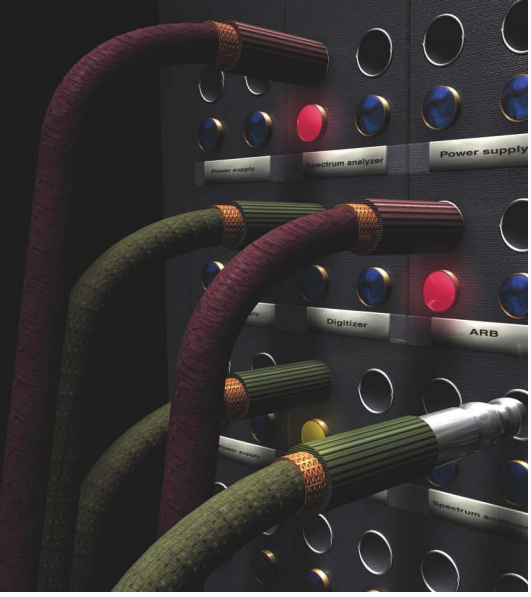

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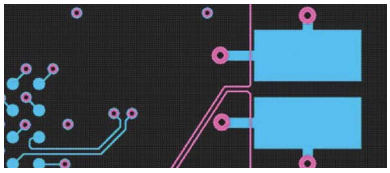
Smooth operators: communicating for communications test

by Rick Nelson, Editor-in-Chief

Industry standards lead push toward energy-efficient computing

by Lee Harrison, Peritus Power

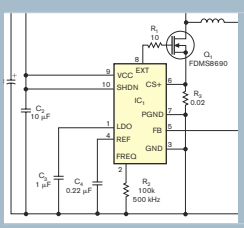


PCB-layout techniques for gigasample ADCs

by Edison Fong, National Semiconductor

pulse

DESIGNIDEAS



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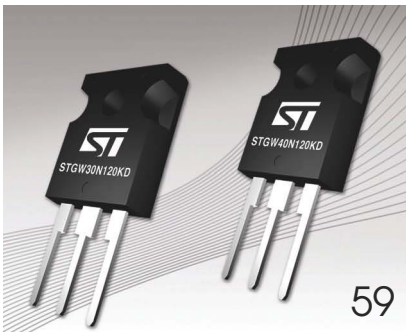

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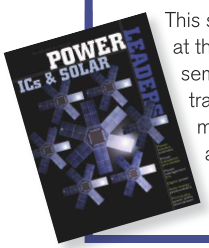
Check out this Web-exclusive article:

Implementing an all-digital PHY and DLL for high-speed DDR2/3 memory interfaces
A new, all-digital approach to implementing high-speed PHY (physical-layer) logic and a DLL (delay-locked loop) offers a path to addressing increasingly stringent market requirements.
→www.edn.com/article/CA6701965

Power Leaders: ICs & Solar



This special section takes a look at the leading vendors in the semiconductor industry for power transistors and diodes, power-management ICs, digital power, and photovoltaics.
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Reed Electronics Group

BY RON WILSON, EXECUTIVE EDITOR

Boeing postpones test flights again: How's your tapeout looking?

Boeing—giant aircraft manufacturer, equally giant but much-lower-profile defense contractor, and one-time paragon of complex project management—has hit the newspapers twice in recent weeks in the worst possible way. The company has announced that it is taking financial charges because neither of its two premier commercial projects—the 787 Dreamliner and the 747-8 cargo version—will meet its most recent schedule for a first test flight. This concern directly affects suppliers providing electronics to those programs. But it is also a cautionary tale for any chip-design team engaged in a complex project.

The irony is that this scenario should happen to Boeing. In the late 1960s, Boeing astonished the aircraft industry by creating the most complex jetliner to date—the initial 747—on a tight schedule and at enormous risk. The company bet essentially its net worth on the 747 project—on a schedule so tight that the first planes for delivery were on the running production line right behind the plane for flight testing and FAA (Federal Aviation Administration) certification. If something had gone seriously wrong, Boeing might have had to rework a year's worth of deliveries in parallel on the factory floor. But the plan—and the plane—worked. The 747 project became a case study in project management and forever altered the landscape of the commercial-aviation market.

That scenario happened when there was limited use of computers and engineers learned manual project-management skills over decades in the must-do environments of World War II, the Cold War, and the Apollo program. Boeing's current disaster is taking place in an environment in which computers control everything. The managers supervising these projects typically have proven expertise in getting a master's degree in business administration, not in getting a project out the door. And this era is one of outsourcing.

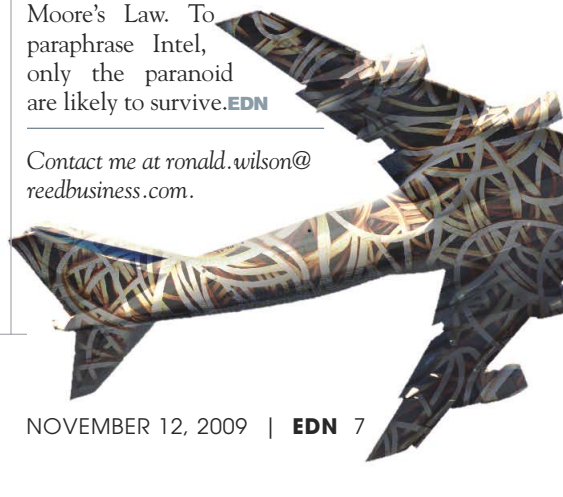
According to published reports, these changes lie at the heart of Boeing's problems. To paraphrase one report, the 787 is an entirely modularized design, and Boeing outsourced the modules. The company intended that final assembly would comprise simply snapping together functionally complete modules, carrying the necessary electronic subsystems, cabling, plumbing, and mechanicals. When the modules started arriving, however, Boeing found that it had somehow lost control of the module designs. In some cases, things didn't fit. In others, module designs exceeded the capabilities of the subcontractors, and so the modules arrived with subsystems missing. Modules required further assembly after delivery. Perhaps more disturbing, no one had, at a full-system level, reality-tested software simulations of the system-level mechanical behavior of the composite materials of which the modules were constructed.

By now, I'm sure this scenario is beginning to sound relevant to chip-design managers. We, too, live in a world of pervasive outsourcing, increasing dependence on simulation at several unlinked levels of abstraction, and no chance of a reality check until someone assembles the complete system. We, too, live in the shadow of the possibility that a system-level design error will become visible only when we flatten the design for physical extraction and DRC (design-rule checking) or during silicon debugging.

In some ways, our problem is more controllable. There are fewer degrees of freedom in even a challenging mixed-signal block than in a physical chunk of a jumbo jet. We have put a lot of investment into tools to manage those degrees of freedom we must accept. And unlike Boeing, no chip-design team is the only one doing what it is doing. (Intel's R&D people are welcome to dispute this point.) So there is a body of experience, however imperfectly we share it.

Yet the caution is still there. It takes only a bit too much confidence in the tools and abstractions; just a little too much casual dealing with the company, language, and time barriers between the core team and the subcontractors; and one step too far down the path of partitioning to turn a challenging project into a catastrophe. The realities of mechanical design and the needs of Boeing's customers place limitations on that company's ambitions. But unlike Boeing, IC-design engineers are all servants of never-ceasing Moore's Law. To paraphrase Intel, only the paranoid are likely to survive. **EDN**

Contact me at ronald.wilson@reedbusiness.com.



Buck regulators with integrated MOS FETs simplify designs up to 25A/phase

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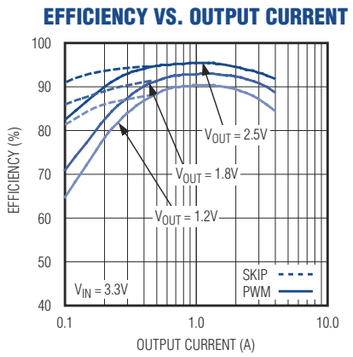

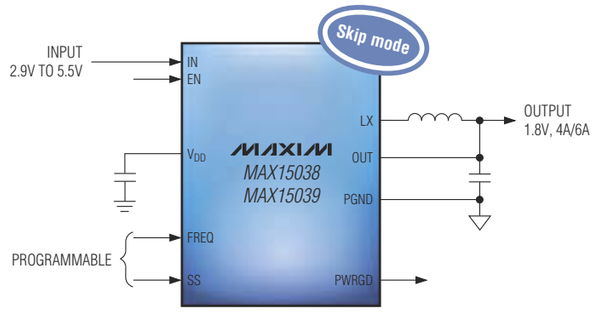

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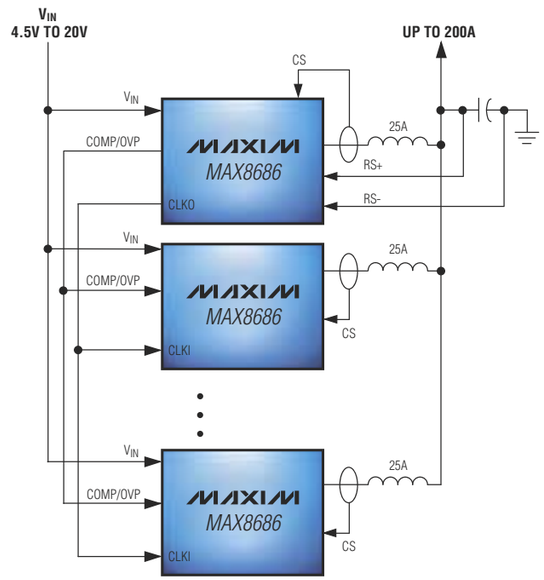

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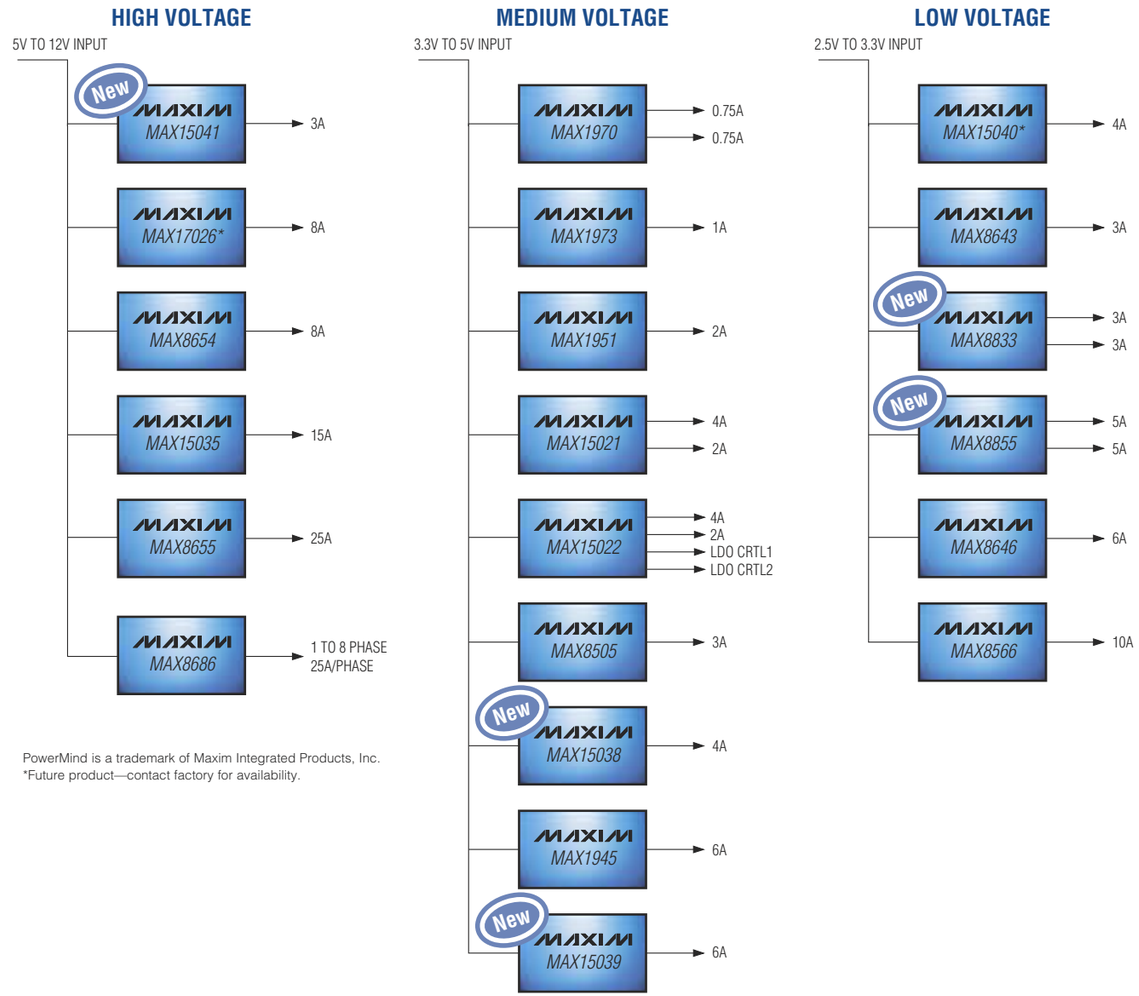

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INNOVATIONS & INNOVATORS

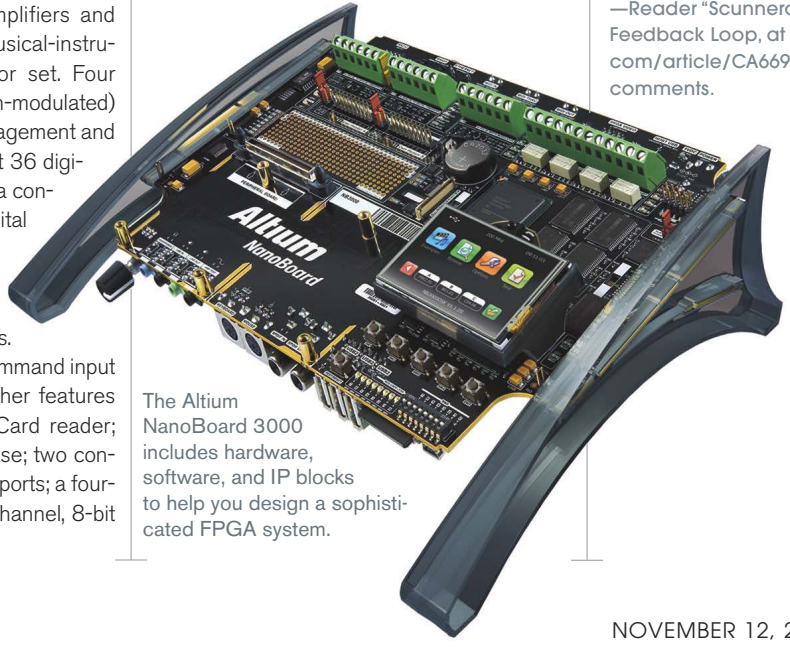
FPGA evaluation boards come with design software

Altium's new NanoBoard 3000 embedded-system development platform includes a board with an FPGA chip, an IR (infrared) remote control, and a 12-month license for Altium Designer schematic and FPGA software. Boards are available for Altera (www.altera.com) Cyclone III, Lattice (www.latticesemi.com) ECP2, and Xilinx (www.xilinx.com) Spartan-3AN FPGAs. The boards come with royalty-free IP (intellectual property) for functions such as a USB (Universal Serial Bus) interface, a TCP/IP (Transmission Control Protocol/Internet Protocol) stack, a touchscreen, a PS2 controller, and SVGA (super-video-graphics-array) capability. The units include three USB ports; an SVGA D-sub connection; eight RGB (red/green/blue) LEDs; and a 2.4-in., 320×230-pixel LCD with touchscreen.

Audio features include a stereo-digital-audio system with onboard power amplifiers and speakers, along with a MIDI (musical-instrument-digital-interface) connector set. Four relays and four PWM (pulse-width-modulated) power drivers provide power management and motion control. Headers bring out 36 digital-I/O pins from the FPGA, and a connector provides access to 50 digital I/Os and to the audio system and power rails. An RJ-45 connecter provides either 10BaseT or 100BaseTX Ethernet connections. An IR receiver lets you provide command input from the remote-control unit. Other features include an SD (secure-digital)-Card reader; PS2 ports for keyboard and mouse; two connectors for RS-232 and RS-485 ports; a four-channel, 8-bit ADC; and a four-channel, 8-bit DAC.

Altium is developing a wireless peripheral-add-on board, for release in December, that supports GSM (global system for mobile) communications, GPS (global-positioning system), and Bluetooth. The Xilinx Spartan-3AN NanoBoard is available now. The Altera Cyclone III and the Lattice ECP2 boards will be available in December. They sell for $395 each, including software, a desktop stand, a speaker-board subassembly, a power-supply module, four power cords for worldwide outlets, a USB cable, an IR remote-control unit with two AAA batteries, an LCD stylus, four jumpers, a volume knob, and an LCD-cleaning cloth. An external enclosure (http://wiki.altium.com/display/ADOH/NanoBoard+3000+Modular+Enclosure) is available for $129.**—by Paul Rako**

▷**Altium**, http://wiki.altium.com/display/ADOH/NanoBoard+3000+Series.



The Altium NanoBoard 3000 includes hardware, software, and IP blocks to help you design a sophisticated FPGA system.

FEEDBACK LOOP

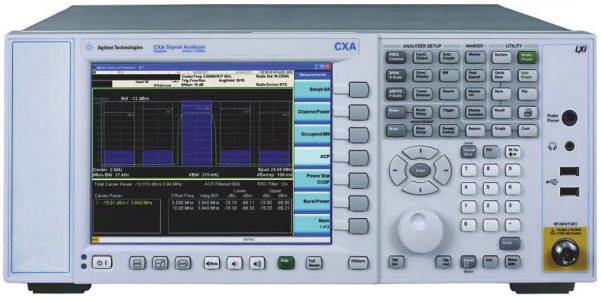
The only reason we're embroiled in this stupid mess is because the (former Federal Communications Commission Chairman Michael) Powell FCC destroyed the common-carrier model, which works so well in the rest of the world. But for that ruling, which gave a monopoly on Internet provisioning to a handful of telephone companies, just because they owned some poles at the side of the road and the metro-cable plant, we wouldn't need to be arguing about 'neutrality.'"

—Reader "Scunnerous," in *EDN*'s Feedback Loop, at www.edn.com/article/CA6699736. Add your comments.

Signal analyzers outshine spectrum-analyzer cousins

Agilent's new N9000A CXA and N9030A PXA series of signal analyzers target a wider niche than do swept-frequency spectrum analyzers. The low-cost N9000A CXA has bandwidths as high as 7.5 GHz, and the high-performance N9030A PXA has bandwidths as high as 26.5 GHz. They offer an array of built-in and optional capabilities that enable them to also perform many tasks that have become critical in testing and evaluating today's complex, digitally modulated communications signals. Both series are part of the manufacturer's larger X-Series, which also includes the EXA and MXA series.

The CXA series' 3- and 7.5-GHz units, whose US base prices range from $12,657 to approximately $16,360, target general-purpose electronics manufacturing, low-cost R&D, and RF education, for which they provide flexibility through built-in and optional measurement capabilities that you can easily reconfigure. The PXA series' architecture supports new measurement applications; future hardware add-ons; wider analysis bandwidths; and possible upgrades to the instrument CPU, memory, disk drives, and I/O ports. The series' models cover frequency ranges of 3 to 3.6, 8.4, 13.6, and 26.5 GHz, and base prices range from $51,900 to $66,300.



Thanks to many built-in and optional features, low-cost CXA and high-performance PXA signal analyzers are more than just swept-frequency spectrum analyzers.

> The PXA is a form, fit, and function replacement for several popular spectrum analyzers.

CXA analyzers offer built-in one-button measurements and optional advanced-measurement applications, including preconfigured test routines for noise figure, phase noise, and analog demodulation. To ensure consistency, the applications are virtually identical to those that run on the EXA, MXA, and PXA analyzers. In addition, the manufacturer's 89600 VSA (vector-signal-analysis) software can run inside the Windows-based instrument, providing advanced analysis of more than 50 demodulation formats. On the production line, the CXA is more than two times as fast as other low-cost analyzers. For example, the CXA can return a peak search result in less than 5 msec and perform a remote sweep and transfer in less than 12 msec through IEEE 488.

The units also include LAN and USB (Universal Serial Bus) 2.0 interfaces. Switching between measurement modes typically takes less than 75 msec. The CXA series offers ±0.5-dB absolute amplitude accuracy, 13-dBm TOI (third-order intermodulation), −157-dBm DANL (displayed average-noise level), and 65-dB-WCDMA (wideband-code-division-multiple-access) ACLR (adjacent-channel-leakage-power-ratio) dynamic range.

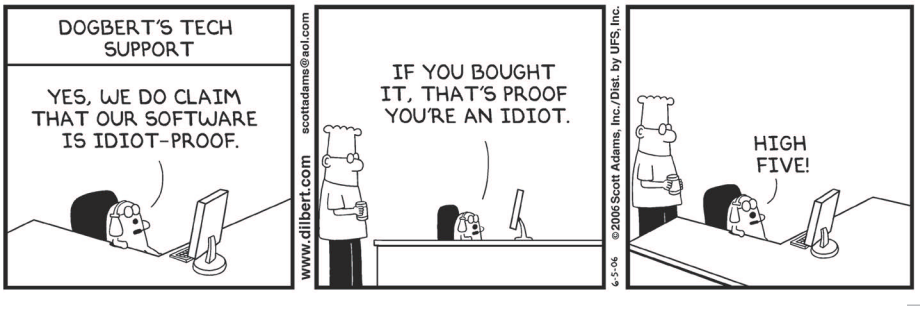
PXA units reduce measurement uncertainty and reveal new levels of signal detail, starting with spurious-free dynamic range as great as 75 dB with 140-MHz analysis bandwidth. Other specifications include −128-dBc/Hz phase noise at 1 GHz with 10-kHz offset, 0.19-dB absolute amplitude inaccuracy, and −172-dBm DANL-based sensitivity at 2 GHz, with preamplifier and noise-floor-extension technology. Like the CXA series, the PXA series offers built-in one-button measurements, optional advanced-measurement applications, and compatibility with other X-Series analyzers and with the manufacturer's 89600 VSA software.

For those looking to easily refresh or replace their test systems, the PXA is a form, fit, and function replacement for several popular spectrum analyzers, including the HP 8566 and 8568; HP/Agilent 856x; and Agilent PSA units whose bandwidth extends to 26.5 GHz. Key features include code compatibility; emulation of remote-programming language; default settings, timings, and couplings; arbitrary and second-IF output; fast-rise-time logarithmic-video output; and Y-axis output. You can purchase The MathWorks' (www.mathworks.com) Matlab data-analysis software directly from Agilent as an option on all X-Series signal analyzers. These packages enable you to make application-specific measurements and test-modulation schemes and to develop customized applications.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/CXA, www.agilent.com/find/PXA, www.agilent.com/find/X-Series_backgrounder.

DILBERT By Scott Adams



RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Bring on the Converter Noise! – Part 1

Q. Is Noise Figure important from the A/D converter's perspective?

A. In terms of the converter, noise figure (NF) and signal-to-noise ratio (SNR) are interchangeable. NF is great for understanding noise density, while SNR measures the total amount of noise in the band of interest. Let's take a closer look at NF though. Some tradeoffs can be misleading, and low NF does not always translate into lower front-end noise seen by the converter.

NF is easy to use in cascaded signal chains when trying to understand the dynamic implications of the design. Remember, that as the source resistance is quadrupled, the NF will improve by 6 dB, but the increased resistance will also increase the Johnson noise that will be seen by the converter. With more source resistance, or half of the full-scale input signal across the converter's analog front-end (transformer, amplifier, or otherwise), noise becomes more difficult to manage over the band of interest, ultimately making the converter's performance worse.

Why is this? If the full-scale input to the transformer or amplifier is lowered, the gain must be increased. This looks fine on paper, for transformers they are more gain-bandwidth dependent than amplifiers. Therefore, optimizing the NF to be as low as possible using a high-impedance ratio transformer, for example, makes it difficult to realize common high-IF applications of 100 MHz and above.

The problem with amplifiers is similar: as the gain of the amplifier is increased the amplifier not only amplifies the signal, it also amplifies its own inherent noise, thus

rapidly degrading the converter's performance. In order to preserve performance, a more complicated (higher order) anti-aliasing filter is required, making it rich with resistive and "lossy" components.

When designing a front-end, keep noise spectral density (NSD) in mind instead. Usually specified in nV/rt-Hz, this is what's really important to the converter, as this is what will be reported and crunched in the digital domain in order to differentiate and ultimately "pick out" the signals of interest within band.

In summary, make sure all the input and output full-scale signals are maximized throughout the signal chain by positioning gain where appropriate. Attenuation, padding, or resistance is not a good NF tradeoff in any signal chain, as it wastes power and increases noise due to resistors. Part 2 will discuss the comparison between resistor noise and converter noise.

A/D Converter Noise Figure equation: NF = Pfs(dBm) + 174dBm – SNR – 10*log (BW). Where Pfs = the fullscale power of the input network used.

To Learn More About the Importance of ADC Noise Figure
http://designnews.hotims.com/23125-101

Contributing Writer Rob Reeder is a senior converter applications engineer working in Analog Devices high-speed converter group in Greensboro, NC since 1998. Rob received his MSEE and BSEE from Northern Illinois University in DeKalb, IL in 1998 and 1996 respectively. In his spare time he enjoys mixing music, art, and playing basketball with his two boys.

Have a question involving a perplexing or unusual analog problem? Submit your question to: raq@reedbusiness.com

For Analog Devices' Technical Support, Call 800-AnalogD

PWM-controller IC operates at temperatures as high as 225°C

Cissoid has introduced the Magma switching-power-supply PWM (pulse-width-modulator)-controller chip, which operates with 6 to 30V inputs and provides duty cycles up to 90%. The device operates at −55 to +225°C, and shutdown current is less than 150 µA at 225°C. You can synchronize the chip to an external clock, and a clock-output pin makes the internal clock available.

Other features include an internal reference, input-voltage feedforward, and a soft-start function when the device comes out of standby or when you enable the outputs. You can adjust the voltage threshold of the power-good output pin.

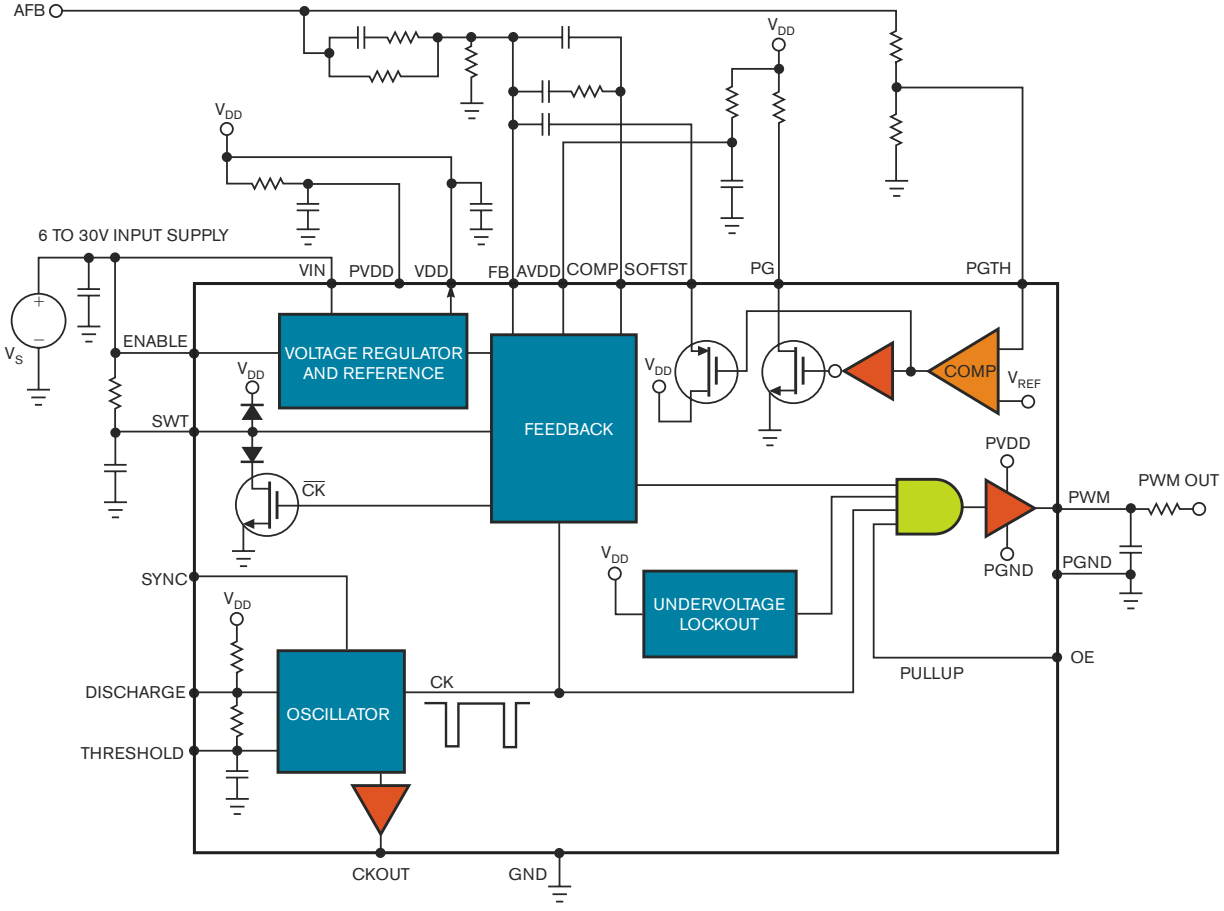
The ceramic package of the Magma PWM-control chip allows it to operate over a −55 to +225°C temperature range.

The device works with the company's Hyperion transistor-driver chip, which also operates at 225°C. This chip set can drive high-temperature silicon-carbide transistors, FETs, or high-reliability IGBTs (insulated-gate bipolar transistors). The parts complement Cissoid's line of regulators, amplifiers, ADCs, logic, and P- and N-channel FETs, all of which operate at temperatures as high as 225°C.

Magma provides PWM control for down-hole oil-well instrumentation, aeronautics, train, and automotive applications. It comes in a ceramic DIL-28 package and sells for $312.70 (200).

—by Paul Rako

▷**Cissoid**, www.cissoid.com.



You can use the high-temperature Magma PWM controller to make regulators and battery chargers that operate at 225°C.

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  - **145 dB (swept-sine)**
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- **Up to 32 Mbyte memory**
- **GPIB and RS-232 interfaces**

FFT analyzers starting at $4950

The SR785 Dynamic Signal Analyzer offers state-of-art performance at a fraction of the cost of competitive analyzers. Standard features include swept-sine mode, order tracking, octave analysis, curve fit/synthesis, and arbitrary waveform source.

When compared to the Agilent 35670A, the SR785 comes out on top. It offers twice the frequency range (2 ch.) and 10 times the real-time bandwidth at less than half the price of the 35670A.

The SR785 is ideal for filter design, control systems analysis, noise measurement, audio or acoustical test, and mechanical systems analysis.

Take a close look at the SR785.

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Device enables remote computer control and management

IT support for computers in remote locations, which include areas as diverse as test equipment, desktop applications, and shopping-center kiosks, often requires the ability to take control of the application's computer over the Internet while maintaining a secure environment. Addressing that requirement, Lantronix has introduced its IPv6 (Internet Protocol Version 6)-certified SpiderDuo KVM (keyboard/video/mouse)-over-IP product. The device provides secure, real-time control of GUI (graphical-user-interface)-based computers, allowing authorized users to perform file transfers, system upgrades, and other tasks and the local port to control local tasks through the computer's keyboard, video, and mouse.

An optional power-control unit provides the ability to remotely control the power to the attached PC, allowing authorized users to initiate system reboots over the network. The power-control unit can put the PC in sleep or power-down mode to save energy, a feature not available with software-only controlling devices. SpiderDuo sells for $380.

—by Margery Conner

▷**Lantronix**, www.lantronix.com.

An optional power-control unit enables the SpiderDuo to remotely control the power to the attached PC.

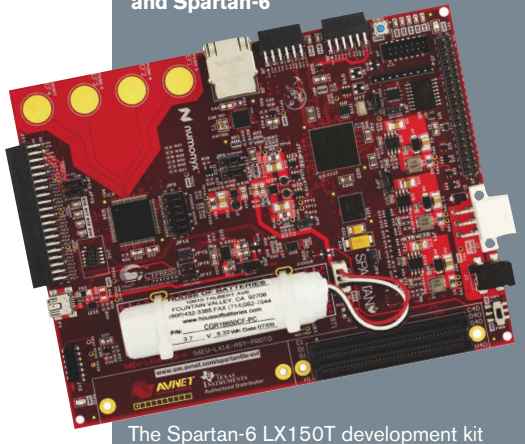
AVNET RELEASES XILINX SPARTAN-6 FPGA EVALUATION AND DEVELOPMENT KITS

The Avnet Electronics Marketing operating group of Avnet Inc has announced the Xilinx (www.xilinx.com) Spartan-6 LX16 FPGA evaluation kit and Spartan-6 LX150T FPGA development kit. Both kits support the new FMC (FPGA-mezzanine-card)-expansion standard, which enables the addition of add-on modules and customization when working with FPGAs.

Avnet based the Spartan-6 LX16 evaluation kit on the Spartan-6 LX16 FPGA. It showcases a system-level approach to low-power design for the Spartan-6 family. Targeting use as a general-purpose FPGA development board, the kit is also suitable for portable instrumentation and battery-powered applications. To emphasize low-power applications, the kit receives its power from an included lithium-ion battery. It can also use a USB (Universal Serial Bus)-cable connection or a 12V adapter and has six high-efficiency portable-power-management ICs from Texas Instruments (www.ti.com). A new PSoC (programmable system on chip) 3 from Cypress (www.cypress.com) adds 20-bit precision analog, system-power management, USB/UART/SPI (serial-peripheral-interface) connectivity, LCD direct drive, CapSense touch sensing, and FPGA-configuration support. The $225 board provides a low-pin-count FMC-expansion connector for adding FMC daughtercards. Avnet plans to begin shipping the kit by year-end. Xilinx will offer a $295-base-price version that emphasizes flexibility.

Employing the Spartan-6 LX150T FPGA with its on-chip 2.5-Gbps transceivers, the kit provides a platform for developing low-cost , high-speed systems. The board features DDR3 memory, a 10/100/1000-GbE (gigabit-Ethernet) interface, and two low-pin-count FMC-expansion connectors; it sells for $995. For more, go to www.edn.com/091112pa.—by Rick Nelson

▶**Avnet, www.em.avnet.com.**



The Spartan-6 LX150T development kit targets video, industrial-networking and -control, wireless-communications, PCIe (Peripheral Component Interconnect Express)-expansion, and general FPGA-prototyping applications.

11.12.09

1-Wire® Advantage

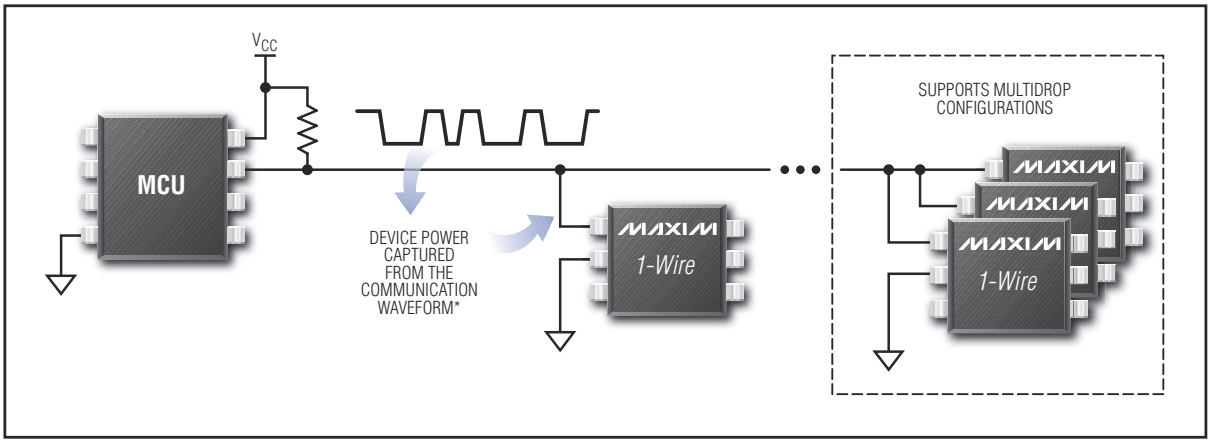
Identify, Authenticate, Locate, and Protect *with 1 Pin*

Customer's Concern

Needs to add or control electronic functionality over a pin-limited connector or processor interface, potentially with a strong ESD performance requirement.

Maxim's Solution

1-Wire devices enable designers to add memory, security, control, and other mixed-signal functions over a single contact, easily and efficiently. ESD performance typically exceeds ±8kV Human Body Model.



How It Works

The 1-Wire bus is a simple signaling scheme that performs serial communication between a host/master controller and one or more 1-Wire slaves sharing a common data line. Both power and data communication for slave devices are transmitted over the single-contact 1-Wire line.

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- **NV Memory for Calibration, Use Tracking, Settings, or Manufacturing Data**
- **Crypto-Strong Authentication Enables**
  - **License Management**
  - **Protection Against NV Data Modification**
  - **Bidirectional Host-Peripheral Authentication, Possibly over a Network**
  - **Clone Prevention**
- **Single or Multipoint Temperature Sensing with Minimal Wiring Complexity/Cost**
- **I/O Sensing and Control**
- **Operation over Pin-Limited Connectors or with I/O-Limited MCU**

*1-Wire devices with special features may require an additional power source.

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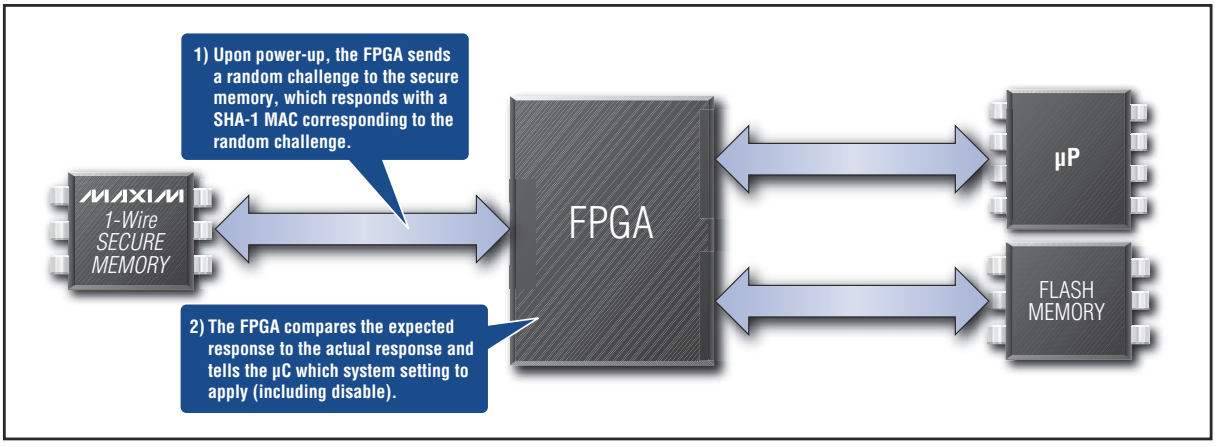
Customer's Concern

Need to securely and cost-effectively protect an FPGA design against unauthorized copying.

Maxim's Solution

Crypto-strong 1-Wire secure memories provide the FPGA design with a proven mechanism to self-test for validity.



How It Works

1-Wire memories utilize a FIPS 180-3 (ISO/IEC 10118-3) Secure Hash Algorithm (SHA-1) to implement a challenge-and-response authentication solution based on a private key. The success or failure of the FPGA authentication sequence is used by the system to set operation or action.

Reference Designs

Easy-to-use reference designs utilizing this cost-optimized copy protection scheme are available by the leading FPGA manufacturers. Visit **www.maxim-ic.com/fpga** for more information.

A Sampling of Innovative 1-Wire Solutions

1-Wire Product Family Function	Customer-Favorite Maxim Device
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Crypto-secure authentication	DS28E01-100: SHA-1 authenticated EEPROM
Temperature measurement	DS28EA00: ±0.5°C accurate digital temp sensor
OTP EPROM	DS2502: 1Kb EPROM
General-purpose I/O	DS2413: 2-channel switch with 28V/20mA GPIO
Unique, 64-bit serial number	DS2401: 64-bit ROM serial number
Real-time clock	DS2417: 32-bit RTC counter

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John Cressler holds a SiGe IC wafer with nanoengineered circuits for use in a space environment.

RESEARCH UPDATE

BY RON WILSON

Team hardens SiGe circuits

Manufacturers once aimed certain process technologies at radiation-hardened designs. CMOS, for example, started out that way, when RCA (www.rca.com) developed its silicon-on-sapphire process. However, the overwhelming success of bulk-silicon CMOS processes has driven most of the alternatives into niches, forcing up their cost to the point that only the best-funded programs can use an alternative process technology to harden their circuitry. That situation leaves everyone else with plain-vanilla CMOS.

As a result, a lot of work over the years has taken place in hardening bulk CMOS. Several foundries offer radiation-resistant processes that, by manipulating the device geometry, reduce the amount of charge that a radiated particle releases as it passes through an IC. Alternatively, these processes could increase the rate of recombination to mop up the charge before it can upset a logic node. In another method, designers use more resistant circuit-design techniques to help reduce either the probability of an upset or its consequences. These measures can take you only so far, however. Circuits that must operate in deep-space conditions, in which they will encounter not only ordinary ionizing radiation but also cosmic rays, also must rely on shielding and redundancy. Both techniques are costly in total mission weight.

Now, John Cressler, a professor at the Georgia Institute of Technology's School of Electrical and Computer Engineering, is leading a team exploring the traditional approach: hardening the process so that the circuits can survive radiation exposure without extensive shielding or redundancy. Cressler's team chose SiGe (silicon germanium) because of its ability to endure exposure to heavy, high-energy particles in cosmic rays. The team first built computer models of the response of SiGe devices to the passage of an ionizing particle through them. The team now intends to use an extremely high-speed oscilloscope to observe the picosecond-level electrical traces of particle impacts and to calibrate the computer models from the hard data. Cressler hopes to then refine device designs to produce a library of SiGe devices that can operate in space conditions without additional process hardening or shielding.

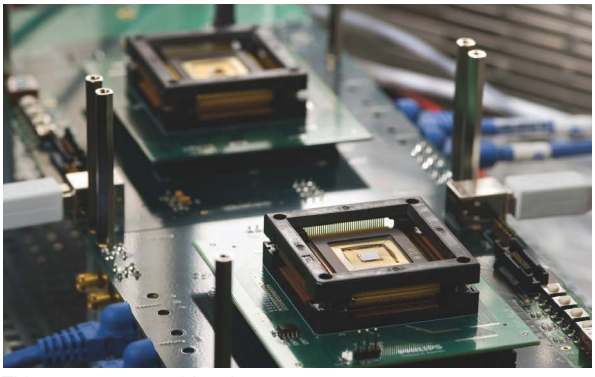
▷**Georgia Institute of Technology**, www.ece.gatech.edu.

Digital photomultipliers challenge vacuum-tube photomultipliers

Despite massive improvements in solid-state light sensors in recent years, the detection of extremely low light levels has remained stubbornly resistant to the incursion of solid-state devices. The problems have been how to deal with the excessive dark count once you integrate the photodiodes into a circuit and how to reduce the cost of the specialized processes that the diodes require. In a paper from last month's IEEE Nuclear Science Symposium and Medical Imaging Conference (www.nss-mic.org/2009/NSSMain.asp), researchers from Philips Electronics claimed to have solved both problems.

Whenever a photon strike or a tunneling or thermal-energy event generates an electron-hole pair, the resulting tiny current pulse goes directly to a high-sensitivity inverter and becomes a digital signal for a counter. The Philips team puts an inverter on each diode and reduces the dark count by disabling any diode/inverter pair that shows excess pulses. An additional circuit on each pair quenches the avalanche photodiode after it has detected a photon and then precharges it to increase its sensitivity for the next arrival, substantially reducing operating power. Philips also integrates the diode, which requires a reverse-bias voltage of approximately 30V, with a low-voltage CMOS process.

▷**Philips**, www.research.philips.com.



This apparatus provides the proof-of-concept test setup for a digital silicon photomultiplier.

BY HOWARD JOHNSON, PhD

Shaping edges

High-speed digital simulations usually begin with a time-domain specification of the driving signal. The specification calls out every moment at which the driving signal, or "excitation," should transition. From that data, the simulation then builds a time-domain sequence or subroutine depicting the excitation as a function of time. As the simulation proceeds, it applies edge shaping to each signal transition.

You can think of the edge-shaping process as a linear filtering operation. For example, pass a perfectly square-edged time-domain signal through a Gaussian lowpass filter, and it produces—guess what—Gaussian edges. Each signal edge looks like the integrated form of a Gaussian bell-shaped curve. You may recognize that shape from statistics as the Gaussian error function, erfc(). Set the Gaussian lowpass filter's −3-dB bandwidth to 0.361/*T*, and it will form signal edges with a 10 to 90% rise and fall time of precisely *T*. This discussion assumes that you have sufficiently separated the signal-transition points to produce a clear and complete copy of the signal edge's shape at every transition.

If you tear apart your simulator code, you may never find an explicit linear signal-filtering routine. There are many ways to make properly shaped signal edges, but they are each equivalent to some linear filtering operation. In every case, the simulator endows the signal with a frequency-response characteristic of the equivalent lowpass filter you used to create the signal edges.

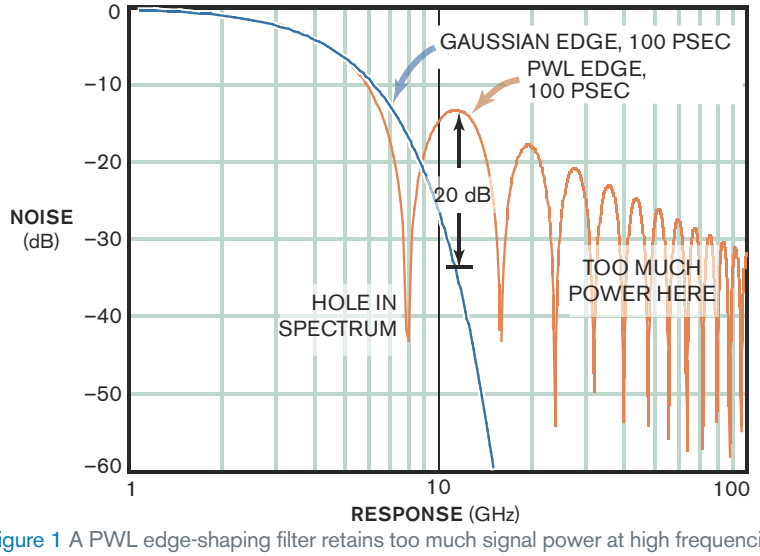


Figure 1 A PWL edge-shaping filter retains too much signal power at high frequencies.

Figure 1 plots the frequency response of two popular edge-shaping filters. The 10 to 90% rise and fall time of each filter is 100 psec. The Gaussian filter exhibits a smooth frequency response with little signal power above 10 GHz. The PWL (piecewise-linear) filter retains an unrealistically large amount of signal power above 10 GHz. This situation happens when you use a PWL function in Spice to create a single linear ramp at each signal edge. Such signals look good on a timing diagram, but they do not represent the spectral qualities of your system.

The PWL filter has a rectangular, or "boxcar," impulse response. When you play a digital signal through a boxcar filter, it creates steps with linear rising and falling edges. If the 10 to 90% rise time is *T*, then the 0=100% rise time must be 1.25*T*. That figure is the actual width of the filter's boxcar response, which accounts for its spectral null at 8 GHz. The sharp corners at the beginning and end of each PWL edge account for the extra signal power at very high frequencies. At 12 GHz, the PWL spectrum peaks some 20 dB higher than the Gaussian spectrum.

I avoid PWL simulation because the PWL edge exaggerates by an order of magnitude the importance of system artifacts around 12 GHz. The PWL edge masks artifacts at 8 GHz because there is no signal energy at 8 GHz to test for such defects. It also vastly overstates crosstalk at high frequencies.

Whenever you need to see details of your actual signal edge shape or spectrum, use a signal-shaping process that properly represents the signals at hand. If you have a record of the actual signal shape or can extract it from an IBIS (input/output-buffer-information) file, use it. In the absence of other information, use a Gaussian shape. EDN

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers. Visit his Web site at www.sigcon.com.

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BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Reference-tool flows and process-design kits, part two

In design support for the fabless or foundry-based semiconductor-design model, the main mechanism for circuit-design information is the PDK (process-design kit). The PDK describes the electrical, yield, and performance aspects of the process. There are generally two types of PDKs: one for device-level or custom design and one for logic-level design. The device-level PDK typically comprises Spice-level device models for all of the active devices available on the process; Spice-level device models for all of the designable passive elements, including resistors, capacitors, and inductors; a schematic-symbol library for these primitive elements; and information on how to build the device in layout.

The Spice models are fairly universal in the semiconductor industry and useful with a variety of simulators, including those for IR (current/resistance) drop; electromigration analysis; postlayout-extraction, high-capacity, mixed-mode simulators such as VHDL-AMS (very-high-speed-integrated-circuit hardware-description-language-analog/mixed-signal) and Verilog-AMS; ac or harmonic-balance RF simulators; and cell-characterization simulators. Spice-level subcircuit models are available for some processes that involve complex elements, such as high-voltage or high-current transistors and metal-insulator-metal capacitors.

The second design view for the custom-design level is for the physical design. It includes the layer list and the technology file for the layout editor and generally references either layouts of the devices to show how to construct a device or an automated program to build the devices from parameterized cells in the language of the layout editor. These parameterized cells are for individual devices, device pairs, and other configurations that the process supports and are available for both passive and active components.

It is no longer always accurate to assume that experienced designers will be working with PDKs.

The parameterized cells tend to be version-specific for a given layout editor and are generally in the design database as "generate-as-needed" elements. Using parameterized cells maintains design flexibility but involves a revision-control risk for the context around the dynamic device. It is common that PDKs omit the reference layouts and parameterized cells for the layouts' nondevice objects, such as guard rings, substrate and well taps, dummy devices, polysilicon or diffusion interconnect, via and contact farms, field plates, line shields, and high-current or high-voltage corner designs.

The next level in the design includes the logic-level PDK. This PDK comprises descriptions for how to set up place-and-route tools, block-to-block-assembly rules, maximum-device-size rules for buffers and repeaters that insert automatically in a design, some schematic symbols for primitive logic elements, and I/Os. The I/Os tend to be special cells that incorporate ESD (electrostatic-discharge)-protection devices, which are process-specific elements. Information for designing these ESD elements is generally proprietary to the foundry. The I/O cells also contain the core and peripheral power-interface circuits. The PDK not only provides these cells but also identifies the proper use and density of the cells a design requires.

First-generation PDKs assumed that a designer using the kits had sufficient design experience and knowledge to properly apply the design information over multiple applications. As a result of the shift to global design centers and the reduction in time designers spend on each process node, it is no longer always accurate to assume that experienced designers will be working with these kits. A proposed method of addressing this issue is to shift to the Python programming language (www.python.com) and the use of that language's multidevice PyCells.

The PyCell device builders include the advantages of adjacent partner devices and their associated nondevice elements. Less-experienced designers may use PyCells with an automated placer to build the device-level IP (intellectual property) and associated cells without requiring the help of senior designers for anything but cell sign-off. EDN

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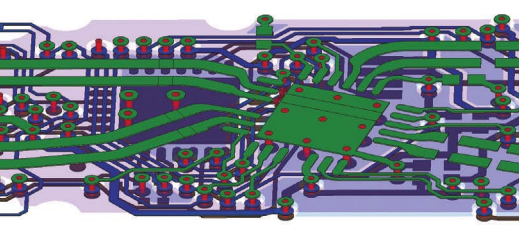

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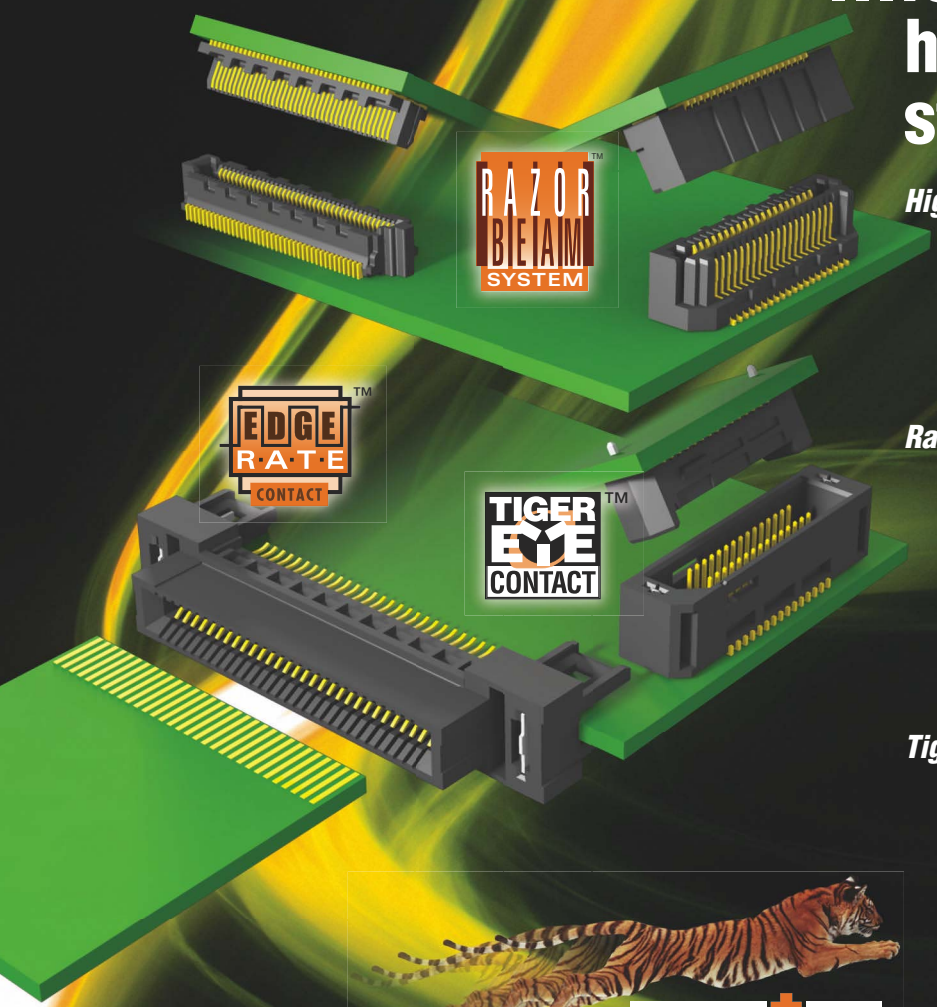

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INDUSTRY STANDARDS LEAD PUSH TOWARD ENERGY-EFFICIENT COMPUTING

ENVIRONMENTAL CONCERNS AND RISING ENERGY COSTS ARE SPURRING INDUSTRY AND GOVERNMENT GROUPS TO DEVELOP REQUIREMENTS FOR HIGH-EFFICIENCY AC AND DC POWER CONVERSION, LEADING TO ENERGY-EFFICIENT SERVERS. MEETING THE NEWEST SPECIFICATIONS WILL DEMAND KNOWLEDGE OF COMPETING POWER-CONVERSION TOPOLOGIES, COMPONENTS, AND DESIGN.

BY LEE HARRISON • PERITUS POWER

In addition to environmental concerns, the increasing cost of electricity is driving data-center managers to more energy-efficient installations. As utility bills become the primary expense for data centers, electricity costs now outweigh real-estate costs, with power consumption per data center ranging from 2 to 22 MW. In 2007, the Internet accounted for 9.4% of total US electricity consumption and 5.3% of global electricity consumption. Networking equipment, such as modems, routers, hubs, and switches, accounted for about 25% of the electricity demand in an average office. If the computers and servers in an infrastructure require 200 kW, then the networking components in that infrastructure need 50 kW. In addition, 45% of the power a data center consumes is for air-conditioning and cooling. In modern data centers, performance per watt has become more critical than performance per processor.

Every year, computers and servers demand higher performance. Server and PC manufacturers respond with larger and faster disk drives, faster memory, multicore processors, and more I/O devices. Although this approach satisfies customer demand, the new designs often require more power and additional cooling, continuing the trend toward higher power consumption. The average power consumption per server has increased from 150 to 250W in 2000 to 450 to 800W in 2009, and the average power per rack of servers in 2000 was nearly 1 kW, rising to 6 to 8 kW in 2006, and should top 20 kW in 2010.

Environmental concerns are not the only ones behind the push to energy efficiency. Electronic equipment that runs cooler has lower failure rates and increased reliability. Data centers save money when servers require less power because less power means decreased cooling and air-conditioning costs. Large data farms benefit from relatively small reductions in electricity cost. Google, for example, may be able to save nearly $1 million a year in utility bills by reducing power consumption by 2 to 3%. Some industry analysts believe that financial benefits are more important than climate issues; in a time of reducing costs across all businesses, this belief may be one factor in the drive toward energy efficiency.

The ac/dc power-conversion step in the overall power chain for server farms can yield some of the most significant gains in power efficiency. Many industry and government groups, including 80 Plus, EPRI (Electric Power Research Institute), the CSCI (Climate Savers Computing Initiative), and the US Environmental Protection Agency, have

developed requirements for high-efficiency ac/dc power supplies. **Table 1** shows the current targets that the CSCI and Energy Star define for single-output power supplies. **Table 2** shows multiple-output supplies (**Reference 1**).

The Silver category is challenging for some power vendors, but the Gold and next-generation Platinum levels are more difficult to reach. Some power-supply vendors have achieved the Gold standard, and some servers are currently available with Gold power supplies, but the Gold standard is unlikely to become well-established until the end of 2010. To meet those standards, manufacturers have taken different approaches, including using interleaved PFC (power-factor control), bridgeless PFC, and resonant topologies.

AT A GLANCE

- The ac/dc power-conversion step in the overall power chain for server farms can yield some of the most significant gains in power efficiency.
- To meet industry standards, manufacturers have taken different approaches, including using interleaved PFC (power-factor control), bridgeless PFC, and resonant topologies.
- Thanks to its 0V switching losses, higher switching frequencies, and smaller footprints, resonant-converter topology may be able to achieve Energy Star Platinum standards.
- For the near future, silicon will remain the dominant switching semiconductor material, and gallium nitride will start to make inroads over the next year.

INTERLEAVED PFC

The power industry has long used interleaving techniques in multiphase-buck-converter designs. This design commonly meets fast load-transient demands for DSPs and other processors. Some designs interleave multiple synchronous power stages to increase power delivery to the load and decrease input and output capacitance, maximizing the benefits of smaller output inductors in each phase of the design. Due to the ripple-current cancellation effects at the output capacitors, this topology can realize transient demands in excess of 350A/µsec.

Interleaving PFC boost stages benefits from the same principles. PFC boost encompasses CCM (continuous conduction mode), DCM (discontinuous conduction mode), and CRM (critical conduction mode). High-efficiency designs are likely to use CCM in the server area because this mode of operation suits power supplies with more than 350W of output power. Although CCM eases the design of EMI (electromagnetic-interference) filters, the approach generally requires a larger boost inductor than do alternative design techniques.

Interleaved CCM is not without its own risks: The design suffers from inherently higher switching and reverse-recovery losses in the rectifier. You can partially overcome these losses, however, by using silicon-carbide diodes. In addition, you cannot typically adjust the frequency in CCM designs because CCM operates as an average-current-mode, PWM (pulse-width-modulated)-control, fixed-frequency design, forcing average input current to be proportional to the rectified ac line cycle.

Energy Star specifications are the primary reason for the move to interleaved PFC. As enclosures and footprints for power become smaller, however, the better EMI performance helps reduce the size of EMI filters. Power density is excellent for interleaved PFC designs, but circuit design can be difficult; the design challenges include its many modes of operation, the need to guarantee safe operation at start-up and shutdown, autoranging of wide-input sources, and fault conditions.

To achieve high efficiency at loads less than 15%, particularly around the 5 to 10% range, you will likely need some form of phase shedding, pulse skipping, or burst modes. These approaches can be fully autonomous or selectable through software and DSPs, depending on load. No matter which approach you choose, problems arise because other functions can be occurring simultaneously. Although using pulse skipping and burst modes lets you attain increased efficiency at light loads, they wreak havoc when you are trying to accurately measure PFC, and they can cause EMI issues and strange harmonic effects in racks and across servers that connect to the same ac source supply.

Measuring PFC at light loads requires the use of a line-impedance-stabilization network and a capacitor between the ac source and the power supply. Investigations are ongoing that aim to reveal the effects of measuring PFC under these conditions. Determining the reason for strange harmonic effects in high-efficiency power conversion also requires further investigation. Thus, efficiency comes at a price. You may be able to improve efficiency, but doing so introduces new side effects.

Implementing PFC in burst or skipping modes also causes problems for the digital-sensing input-voltage, -power, and -current outputs. Although fully digitally controlled power supplies can likely cope with these problems, it's difficult to obtain valid data from a control signal that is constantly changing. Many designs turn off power reporting at these lighter load conditions, but Energy Star is determined to tighten the already difficult-to-meet specifications, so designers must find approaches for reporting data at light loads. Digital techniques in PFC have recently produced impressive performance at light loads but at the expense of THD (total harmonic distortion).

BRIDGELESS PFC

Bridgeless PFC offers loss savings of 0.4 to 1.5W at high-load conditions,

TABLE 1 TARGETS FOR SINGLE-OUTPUT POWER SUPPLIES

	CSCI Silver and Energy Star Version 1			CSCI Gold and Energy Star Version 1			CSCI Platinum		
Loading (%)	Efficiency (%)	PFC (≤1000W)	PFC (>1000W)	Efficiency (%)	PFC (≤1000W)	PFC (>1000W)	Efficiency (%)	PF (≤1000W)	PF (>1000W)
10	75	0.65	0.8	80	0.65	0.8	82	0.65	0.8
20	85	0.8	0	88	0.8	0.9	90	0.8	0.9
50	89	0.9	0.9	92	0.9	0.9	94	0.9	0.9
100	85	0.95	0.95	88	0.95	0.95	91	0.95	0.95

TABLE 2 TARGETS FOR MULTIPLE-OUTPUT POWER SUPPLIES

	CSCI Bronze		CSCI Silver		CSCI Gold	
Loading (%)	Efficiency (%)	PFC	Efficiency (%)	PFC	Efficiency (%)	PFC
20	82	0.8	85	0.8	87	0.8
50	85	0.9	88	0.9	90	0.9
100	82	0.95	85	0.95	87	0.95

depending on output power. The benefits of a low-power-line mode are much greater and suit countries that still run servers in low line conditions. Standard bridge rectifiers suffer in this application because they use series-connected semiconductors, but the approach remains a low-cost and reliable choice for ac rectification. In some designs, standard bridge rectifiers run at dangerously high temperatures. Airflow is typically not ideal in the location of a 1U server power supply, and some customers of power-semiconductor manufacturers have requested an increase in thermal capabilities to 175°C from the previous limit of 150°C.

Bridgeless approaches have not become mainstream designs due to their higher cost and challenges, including complex gate-drive circuits and the difference between the input and the output ground references. Prototypes of bridgeless designs have shown high-EMI common-mode switching elements at the negative bulk-capacitor connection, and, with virtually no low-frequency path back to the ac source, EMI is greater. Various semiconductor companies, including STMicroelectronics and On Semiconductor, now offer controllers for bridgeless rectification, although some operate only in high line conditions. These units operate at fixed frequencies of approximately 100 to 150 kHz, but the $20 to $60 cost to implement bridgeless front ends is too high for a 1W power saving.

For now, CCM designs with carefully used silicon and light-load power-saving techniques have sidelined bridgeless designs. Unless there is a major breakthrough in the cost, complexity, and confidence of bridgeless technology, this scenario may remain so for some time to come. In addition, if dc-based power-distribution infrastructures for data farms become popular, ac/dc bridgeless technology may become obsolete before it gets off the ground.

RESONANT TOPOLOGIES

Thanks to its 0V switching losses, higher switching frequencies, and smaller footprints, resonant-converter topology may be able to achieve Energy Star Platinum standards. Moreover, parasitics, which are problematic for alternative topologies, become advantageous in resonant topologies (**Table 3**). PWM designs lose power at high switching frequency, and resonant-mode topology begins where PWM topologies end. There are many options available in waveform shaping to eliminate switching losses, including ZCS (zero-current switching); ZVS (zero-voltage switching); and quasiresonance, which uses only a part of the sinusoidal waveform.

Power designers commonly choose

TABLE 3 COMPARISON OF RESONANT POWER SUPPLIES

Converter	Advantages	Disadvantages
Series resonant	Behaves as a current source and best suited to high-voltage, high-power designs Provides good handling of overload and fault conditions Requires small or no output filter	Poor regulation at light- and no-load conditions Continuous-current mode below resonance causes high component stress and premature failure if not carefully designed
Parallel resonant	Behaves as a voltage source and suitable for low-voltage outputs, good no- and light-load regulation Discontinuous mode of operation is similar to standard PWM buck conversion	Requires snubbers, consuming efficiency Does not self-protect in overload or short-circuit conditions, requiring additional protection Constant resonant circulating current at all load conditions can cause problems
Zero-current switching, quasiresonant, fixed on-time	Low turn-off losses in silicon Recycles any remaining leakage current	Power components contain high peak currents
Zero-voltage switching, quasiresonant, fixed off-time	Virtually eliminates switching losses Recycles any remaining leakage current	Operates above resonant range Power devices require at least three times the supply voltage; multiresonant techniques offset this problem
Series-parallel resonant	Excellent performance at light-load, no-load, and short-circuit or fault conditions	Produces parasitic elements that can be troublesome, requiring additional passive components
Multiresonant, zero-voltage-switching Class E	Virtually eliminates switching losses, virtually no frequency shift compared with other methods	Can cause stability issues and generates high peak voltage and current across semiconductors
Clamped PWM	Simple control loop with low-voltage stress Current-mode capable and fixed frequency of operation	Turn-on losses can be high; operates best at medium- to full-load conditions
PWM, zero-voltage switching	Fixed-frequency design with maintained switching losses at low levels across all power devices High efficiency at high switching frequency	Creates problematic switching noise at light loads and does not achieve zero-voltage switching in the light-load mode of operation
LLC resonant	High efficiency with excellent line/load regulation Outperforms series-resonant mode	Performance is superior to other modes of operation, but design is critical Possible N+1-redundancy concerns

LLC (inductor-inductor-capacitor) converters to implement resonant topologies. These devices offer good regulation and frequency control, and they boast efficiency as great as 97% for the LLC stage, further assisting compliance with the Platinum standard. LLC topologies also have reduced inductance in the primary transformer, excellent frequency control over a wide load range, excellent line and load regulation down to zero loads, and ZCS control of secondary rectifiers.

MATERIAL AND MAGNETICS

For the near future, silicon will remain the dominant switching semiconductor material, and gallium nitride will start to make inroads over the next year (**Reference 2**). Gallium-nitride promises a tenfold reduction in on-resistance for 50V devices by 2013, but no more than 10% of applications will be widely implementing it before 2015. Using planar transformer technology and integrated magnetics with power components as part of the transformer assembly can achieve 0.5 to 2W savings. Planar magnetics offer lower switching and copper losses. They also offer a low profile, high power density, and high frequencies, so designers can build them into the main PCB (printed-circuit board) or assemble them as subassemblies for daughtercards.

Integrated magnetics can provide a 50% smaller footprint than you can achieve using separate magnetic and rectification stages. Thanks to lower commutation loops, the approach also offers lower, better-controlled high-frequency power-supply noise spikes and EMI, and reduced copper losses guarantee increased efficiency. Generally, integrated magnetic designs offer repeatability and cost reductions in manufacturing, and the tolerances of magnetic characteristics and output stages show closer results to each other than those of discrete stages. This technology will find its way into future high-efficiency designs; the option of increased power density alone is a big enough reason to adopt the technology. Efficiency gains may even become secondary to this requirement.

The magnetics industry has seen fewer improvements in technology than the semiconductor industry. Passive components account for more than 75% of power-supply real estate; you must target these components when looking to reduce your design's size and increase its power density. Magnetic components, including EMI filters, account for the biggest real-estate consumer, and bulk-capacitor electrolytics follow closely.

DIGITAL CONTROL

Digitally controlled power supplies have seen improvements in efficiency due to improvements in digital control and optimization and sensor accuracy for voltage and current reporting from the power supply. The recently released Energy Star requirement requires ±10% accuracy with a cutoff at ±10W—that is, the accuracy need never be better than ±10W. The Tier 2 specification, which will come out in October 2010, will require ±5% accuracy with a cutoff at ±5W, making this requirement one of the most difficult to meet. The voltage-reporting accuracy is relatively easy, but the current-reporting accuracy is difficult because the sensing component must have an extremely low value to

avoid consuming additional power and thus lowering efficiency. Further, at low loads, the current waveform for determining the current reporting is too distorted to be meaningful. You typically use the PFC current to sense input current. SNRs (signal-to-noise ratios) can be poor, and it is not unusual to need signal amplifiers to improve the signal. However, in digitally controlled power supplies, the DSP can calibrate the current-sensing element. You typically use a rectifier separate from the main power rail to sense input voltage. A primary-side DSP using power-correction factors can sense peak or average voltages and report the status. The accuracy you can achieve with this technique ranges from 1 to 5%.

FOR MORE INFORMATION

80 Plus
www.80plus.org

Climate Savers Computing Initiative
www.climatesaverscomputing.org

Electric Power Research Institute
www.epri.com

Energy Star
www.energystar.gov

Environmental Protection Agency
www.epa.gov

On Semiconductor
www.onsemi.com

STMicroelectronics
www.st.com

You can report input power as a function of input current and input voltage. Again, designers typically use calibration to prevent errors, and you must build the aging of components into this calibration. Without digital filtering and carefully controlled algorithms, these requirements would be almost impossible to meet. Even with today's technology, it is a difficult task.

Digital control assists not only with the latest energy-sensor-reporting requirements but also with the control of power conversion and optimization of efficiency. It allows direct control over phase control, burst or skipping modes, switching-frequency control, transient response, voltage and current limits, dead times, and sequencing of internal waveforms and voltages. Optimization of switching frequencies is a complex task, which becomes a four-way juggling act involving power-supply performance, efficiency, magnetic-component footprint sizes, and power-supply-enclosure limitations. **EDN**

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2. Brier, Michael A, "GaN Based Power Devices: Cost-Effective Revolutionary Performance," International Rectifier, 2008, www.irf.com/pressroom/articles/560PEE0811.pdf.

AUTHOR'S BIOGRAPHY

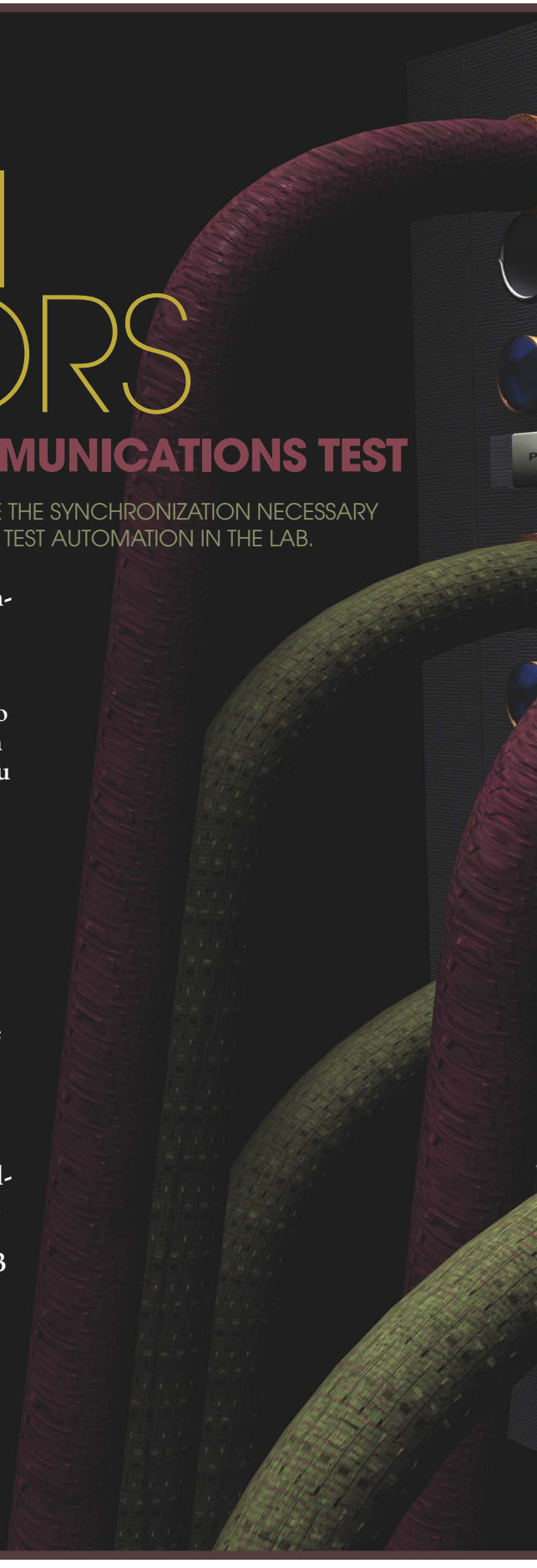
Lee Harrison is director of Peritus Power (www.perituspower.com). Previously, he worked at Sun Microsystems as a power-system architect and technical leader for the Sparc and x86 platforms, developing the technology and strategy for power conversion with Emerson Network Power, Delta, Lineage, Power One, and FDK from 2000 to 2009. He provides input to the Environmental Protection Agency on power-related issues and has been a voting member of the Climate Savers ac/dc work group for the last four years. Before joining Sun, Harrison was an engineering manager for a UK-based defense power-supply company, specializing in high-density, low-profile dc/dc and ac/dc power conversion and nuclear-protected electronics. His LinkedIn profile is located at www.linkedin.com/pub/lee-harrison/0/382/569.

BY RICK NELSON • EDITOR-IN-CHIEF

SMOOTH OPERATORS

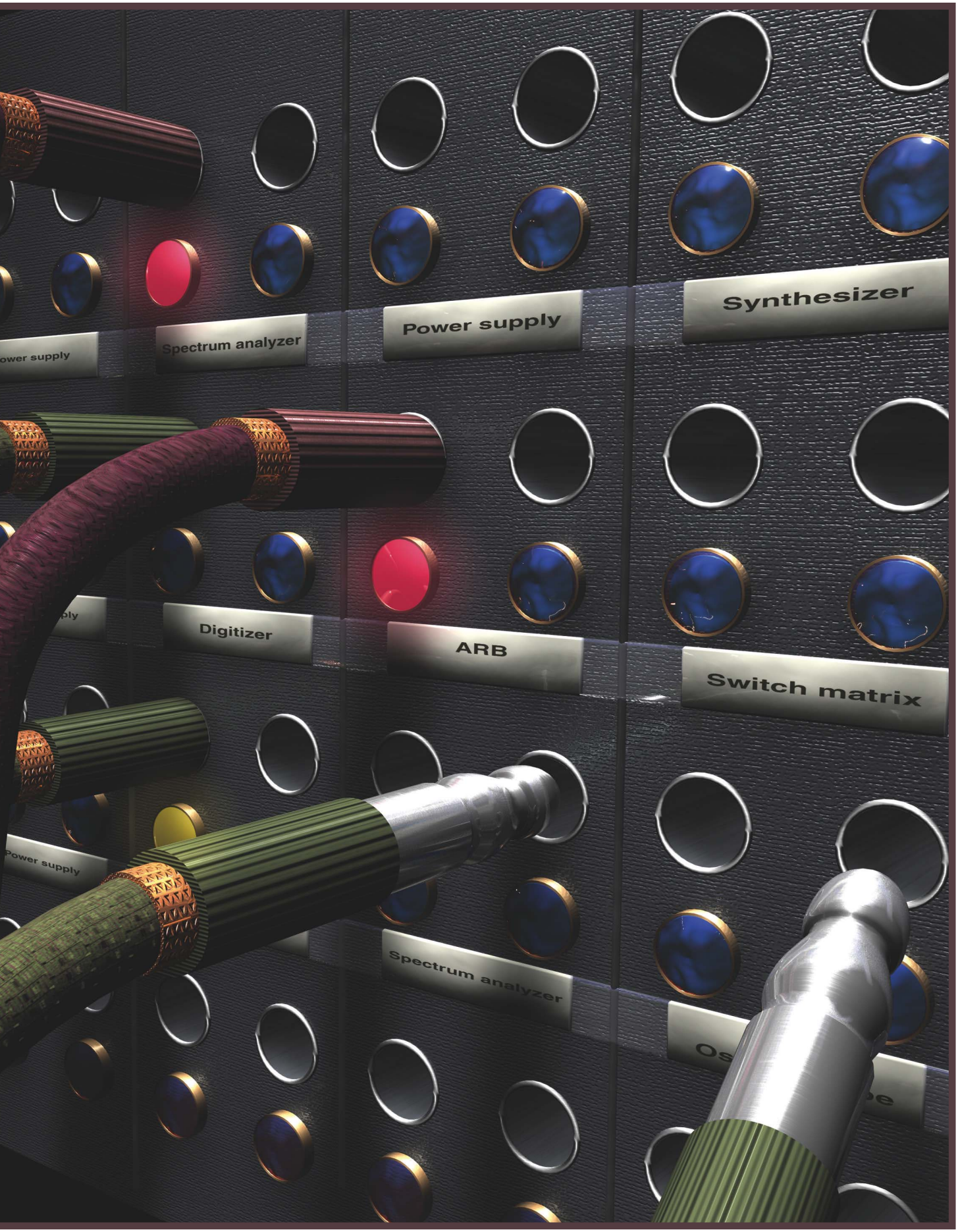
COMMUNICATING FOR COMMUNICATIONS TEST

LXI AND PXI INSTRUMENTS AND RELATED SOFTWARE PROVIDE THE SYNCHRONIZATION NECESSARY FOR MAKING COMPLEX MEASUREMENTS, AND THEY ENABLE TEST AUTOMATION IN THE LAB.



When you're designing complex devices and systems for communications and other sophisticated applications, you often need to make measurements with instruments that can talk to each other. You might, for instance, need to synchronize a signal source and an analyzer to evaluate a prototype, or you may need to make automated measurements to collect voluminous characterization data.

Instruments have long been able to communicate with controllers and with each other to serve such applications. That capability dates back to the late '60s, to the invention of the HP-IB (Hewlett-Packard interface bus), codified as the IEEE-488 standard and taking the vendor-neutral name of GPIB (general-purpose interface bus). And instruments have long been available with general-purpose computer-centric interfaces ranging from RS-232 to USB. But those interfaces have limitations. GPIB cables are bulky and expensive, and data rates are limited. USB cables are ubiquitous and cheap, but the interface has no instrument-specific features and limits you to communications with a few instruments near a single computer.


Spectrum analyzer
Power supply
Synthesizer
Digitizer
ARB
Switch matrix
Spectrum analyzer

The LXI (local-area-network-extensions-for-instrumentation) and PXI (PCI-extensions-for-instrumentation) standards are overcoming these limitations. The standards' respective proponents, which the LXI Consortium (www.lxistandard.org) and PXI Systems Alliance (www.pxisa.org) represent, touted each standard's features and benefits at industry events during the summer and fall. You can use instruments conforming to either standard alone or in hybrid systems to bring automated test capability to your laboratory. Indicating that there is no single correct instrument-system architecture for every application, several vendors are supporting or are at least investigating both standards (highlighted in **Table 1**).

If you are working in the microwave range, you'll need an LXI system or a hybrid system with LXI-microwave instruments. In the PXI format, Phase Matrix Inc offers the 26.5-GHz PXI-1420 downconverter, and Pickering Interfaces offers PXI microwave switches. However, general-purpose PXI RF signal sources and receivers, from Aeroflex and National Instruments, top out at 6 and 6.6 GHz, respectively. Rather than looking to boost bandwidth, makers of PXI RF modules have been targeting support for emerging technologies. Aeroflex, for example, recently announced new LTE (long-term-evolution) measurement capabilities for its PXI systems. In contrast, just about any type of instrument you can buy for the bench top is probably available in an LXI-compliant version. For example, Rohde & Schwarz just introduced its R&S ZVA67, a 10-MHz to 67-GHz vector network analyzer. The instrument complies with LXI Class C.

In addition, LXI can prove to be the technology of choice if you require some form of remote access or if you must cover long distances. For example, if you need to conduct tests on a radar range in which your source and receiver are hundreds of meters apart from each other, an LXI system can easily accomplish measurements that would otherwise be impractical (**Reference 1**).

On the other hand, PXI affords a way to easily configure an instrument system without dealing with LAN issues and without involving your IT department. PXI inherently provides clock synchronization among instruments in a backplane—an ability available on LXI Class B and C instruments but not on the more common—particularly in the RF and microwave range—Class C versions. Further, PXI systems can stream data at high rates for off-instrument storage and analysis.

AT A GLANCE

- Instruments' ability to communicate with controllers and with each other dates back to the late '60s, to the invention of the HP-IB (Hewlett-Packard interface bus), codified as the IEEE-488 standard and taking the vendor-neutral name of GPIB (general-purpose interface bus).
- PXI (PCI-extensions-for-instrumentation) and LXI (local-area-network-extensions-for-instrumentation) standards are overcoming the limitations of HP-IB and GPIB.
- In the PXI approach, the modules are inherently synchronized simply because you put them in the same chassis.
- LXI products cover every major product category for building a high-performance test system, with no holes or gaps in instrument capability.
- Ultimately, there will be room for a variety of instrument formats.

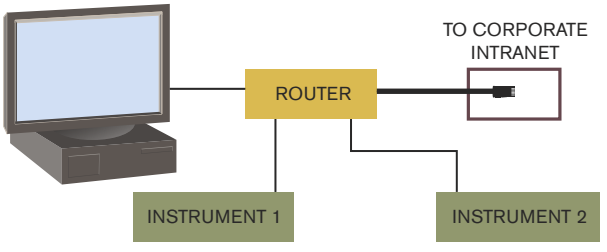


Figure 1 You can buy a router to connect your PC and your LXI instruments to your corporate network in a way that won't upset your IT department, according to Chris Van Woerkom of Agilent Technologies.

MAKING THE CASE FOR LXI

"Today, 1211 products are certified as LXI-compliant, approximately a 50% increase from 12 months ago," said Agilent Technologies' Von Campbell, who serves as the LXI Consortium's president, speaking Sept 16 at Autotestcon. Over the same period, he said, instrument families available with LXI connectivity increased from 64 to 140, with 24 member companies having LXI-compliant products. He noted that LXI products cover every major product category for building a high-performance test system, with no holes or gaps in instrument capability.

Joining Campbell at the Autotestcon LXI presentation were Rob Purser, manager for test-and-measurement products for Matlab and Simulink at The MathWorks; Bob Stasonis, sales and marketing manager at Pickering Interfaces; Chris Van Woerkom, senior marketing engineer at Agilent Technologies; and Tom Sarfi, vice president of business development at VTI Instruments.

Purser noted that LXI "leverages the telecom wave" to reduce interconnect costs and ensure long-term stability for your test system. Ethernet, he said, has a 30-year history of evolution and maintains compatibility. Most LXI implementations don't require special hardware, although Purser cautioned against buying the cheapest Ethernet cables for your instrument system. He said LXI complements current technologies, allowing you to use LXI with your GPIB, PXI, or VXI (Versa Module Eurocard-bus-extensions-for-instrumentation) system.

Despite the capabilities of Ethernet, Purser said, Ethernet alone is not enough. If you use Ethernet alone—and many instruments do have Ethernet interfaces—you'll need a way to configure hundreds of LAN options, to discover instruments, to connect test-and-measurement software to instruments, and to coordinate measurement activities. LXI, he added, provides a standard default-LAN configuration to handle the details you would otherwise have to deal with when connecting your instruments to a LAN. To show how easy it can be to set up an LXI system, Purser at The MathWorks' Autotestcon booth demonstrated a communications-channel test setup comprising Agilent and Tektronix instruments operating in conjunction with a PC running MathWorks' Matlab software.

Van Woerkom of Agilent elaborated

on LXI's capabilities, noting that it provides a consistent set of LAN-communication services for test systems, supports LAN discovery for instruments, defines a standard Web page for instruments, specifies IVI (Interchangeable Virtual Instrument) drivers, requires interoperability testing for compliant products, and offers extensions for triggering and synchronization.

DEALING WITH YOUR IT DEPARTMENT

If you've ever dealt with your IT department, you might believe that LAN connectivity is a bug and not a feature. Speaking during the Autotestcon presentation, Stasonis of Pickering Interfaces commented on how to avoid pitfalls when connecting instruments to a corporate network and offered advice on dealing with firewalls and your IT department, which, he said, is understandably concerned with uptime and security issues.

If your automated-test-system requirements are modest, you might get by with a configuration that won't upset your IT department, said Van Woerkom. He described a system with a PC, a router, and LXI-compatible instruments configured in an isolated subnet (**Figure 1**). You can let your router configure your instruments using the DHCP (Dynamic Host Configuration Protocol), although manually assigning IP (Internet Protocol) addresses and aliases can avoid problems associated with address reassignment and simplify programming. "Programs like a fixed address," he said.

If you must communicate with instruments across a campus or around the world or if you want to provide remote access to the instruments in your lab, IT involvement is essential. According to Stasonis, you'll need to identify the number of IP addresses you need, define a network topology that minimizes latency and simplifies discovery, and describe your anticipated network traffic with respect to bandwidth and the services and protocols you'll be using. In addition, he said, you will want to determine where you archive test results and how to handle system updates—of virus protection, for example.

To conclude the Autotestcon presentation, Sarfi of VTI Instruments outlined the instrument characteristics of classes C, B, and A. Class C is the basic configuration, ensuring interoperability with other LXI Class C instruments. Most LXI-compliant RF and microwave instruments fall into Class C, although VTI makes Class A-compliant microwave switches. Class B instruments implement the IEEE 1588 standard to provide synchronization among instruments, each of which includes its own clock operating at a slightly different rate from its neighbors. Class B systems include one timekeeping master and several slaves, using time stamps to keep clock deltas in the 10s of nanoseconds, Sarfi said. He concluded by describing Class A instruments, which include an eight-lane M-LVDS (multipoint-low-level-differential-signaling) bus to support precise asynchronous handshaking at hardware speeds, with errors limited to propagation delays.

(Note that *EDN* sibling publication *Test & Measurement World* presented a Webcast version of the Autotestcon presentation on Oct 13. You can view an archived version of the Webcast at www.tmworld.com/webcasts.)

FROM BENCH TOP TO PXI

If you plug all your instruments into one backplane, you have no need for IEEE 1588 synchronization or a separate hardware

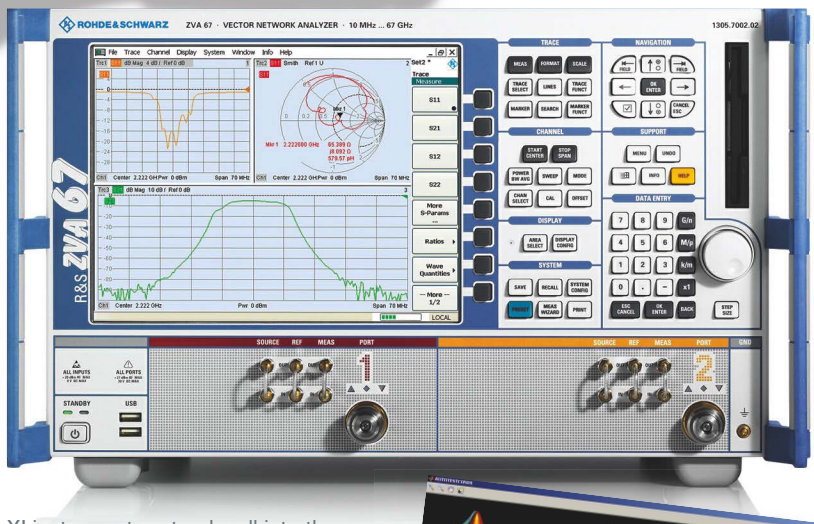
TABLE 1 KEY MEMBERS OF THE LXI CONSORTIUM AND PXI SYSTEMS ALLIANCE

Company	LXI	PXI
Adlink Technology, www.adlinktech.com		•
Aeroflex, www.aeroflex.com	•	•
Agilent Technologies, www.agilent.com	•	•
Alfautomazione, www.alfautomazione.it		•
Ametek Programmable Power, www.elgar.com	•	
Averna, www.averna.com		•
BAE Systems, www.baesystems.com		•
Brüel & Kjaer, www.bksv.com	•	
C&H Technologies Inc, www.chtech.com	•	A
Chroma ATE, www.chroma.com.tw		•
EADS North America Defense, www.eads-nadefense.com	•	A
Geotest, www.geotestinc.com		•
Gigatronics, www.gigatronics.com		•
Goepel Electronic, www.goepel.com	•	•
IPTE, www.ipte.com	•	
Keithley Instruments Inc, www.keithley.com	•	A
Kepco Inc, www.kepcopower.com	•	
LeCroy, www.lecroy.com	I	•
MAC Panel, www.macpanel.com		•
MathWorks Inc, www.mathworks.com	•	
National Instruments, www.ni.com	•	•
One Stop Systems, www.onestopsystems.com		•
Pacific MindWorks, www.pacificmindworks.com	•	
Phase Matrix Inc, www.phasematrix.com		A
Pickering Interfaces Ltd, www.pickeringtest.com	•	•
Rohde & Schwarz GmbH, www.rohde-schwarz.com	•	A
TDK-Lambda Americas Inc, us.tdk-lambda.com	•	
Tektronix, www.tektronix.com	•	O
Teradyne, www.teradyne.com	I	•
Virginia Panel, www.vpc.com		•
VTI Instruments Corp, www.vtiinstruments.com	•	
ZTec Instruments, www.ztec-inc.com	•	•

This list includes companies mentioned in this article as well as LXI Consortium strategic, participating, and advisory members and PXI Systems Alliance sponsor and executive members. It does not include informational or associate members of the respective organizations unless noted. The highlighted companies participate in both organizations or have otherwise signaled their interest in both standards. Visit www.lxistandard.org and www.pxisa.org for more information.

Notes

A=associate member of the PXI Systems Alliance
I=informational member of the LXI Consortium
O=Tektronix is working with National Instruments to develop a PXI oscilloscope that will incorporate Tektronix technology and be marketed by National Instruments

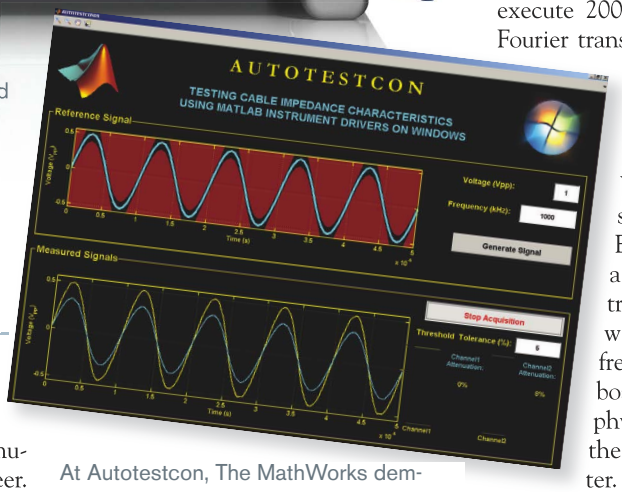


LXI instruments extend well into the microwave region. A recently introduced example is the Rohde & Schwarz R&S ZVA67, a 10-MHz to 67-GHz vector network analyzer that is LXI Class C-compliant. The instrument features a 110-dB dynamic range at 67 GHz and can serve in R&D as well as production applications.

bus. "Suppose you want to synchronize two digitizers," said David Hall, National Instruments' RF-and communications-product-marketing engineer. "In the old oscilloscope approach, you connect some cables on the back. With the PXI approach, you just say 'use PXI trigger line 1,' and that's all there is to it. From a timing and synchronization point of view, there are some inherent advantages to all the modules having access to a common digital bus." Hall elaborated on PXI's benefits for communications system design, particularly for measurements involving MIMO (multiple-input/multiple-output) radios. With traditional instrumentation, he said, "The way you would make those measurements is you would buy two vector signal analyzers and connect cables on the back end and hope that the LOs [local oscillators] are synchronized. In the PXI approach, the modules are inherently synchronized simply because you put them in the same chassis."

Hall cited another communications example. Attendees at ION GNSS 2009, the Institute of Navigation's Global Navigation Satellite System meeting, which took place Sept 22 through 25 in Savannah, GA, were attempting to build better GPS (global-positioning-system) receivers. As part of their efforts, Hall said, they take PXI systems into the field and acquire raw satellite signals from the air. The PXI backplane is both a command bus and a data bus, and PXI Express can stream acquired I/Q (in-phase/quadrature) samples in real time "until you fill up a hard drive," he explained. You can then use the stored samples to exercise and optimize prototype receivers.

To emphasize NI's commitment to ensuring that PXI hardware, along with NI's LabView, can serve communications applications, NI fellow Mike Santori said at an Aug 5 NIWeek presentation that NI had created an internal R&D team of communications experts.



At Autotestcon, The MathWorks demonstrated the test of cable impedance characteristics using Matlab software and LXI-compliant instruments from Agilent and Tektronix.

To put the NI hardware and software through its paces, team members developed an LTE base-station emulator.

Team member Ian Wong, a senior RF-communications-software engineer at NI, brings to the team academic and industry experience in meeting communications-design challenges. For NIWeek attendees, Wong described the challenges that LTE presents (**Reference 2**). LTE, he said, when it rolls out next year, will support 300-Mbps data rates, versus 500 kbps for the EDGE (enhanced-data-for-global-system-for-mobile-communication-evolution) technology in common use today. An LTE base station will execute 200,000 2048-point FFTs (fast Fourier transforms) per second and will include a 300-Mbps turbo decoder, all adding up to performance of trillions of operations per second. Wong's team built the base-station emulator using a PXI Express system that includes a real-time dual-core controller, which communicates with a PXI IF (intermediate-frequency)-transceiver FPGA board that in turn performs physical-layer processing for the LTE base-station transmitter. A PXI RF upconverter delivers the output to a device under test. Signals from that device are routed to an RF downconverter and on to the IF-transceiver FPGA board.

A MATTER OF TASTE

If you are a bench-top-instrument user in an application that both LXI and PXI can serve, your choice of platform when moving to automation may center on your experience, your comfort level, and your age. Hall at NI said that he learned to use an oscilloscope in college, and the point was for the instrument to provide him with diagnostic information that would enable him to make decisions. With the proliferation of PCs into test applications, it becomes important to get measurement information into a PC and use the PC to control the instruments and assist in decision-making. Although LXI and GPIB permit automation of bench-top instruments, "that wasn't the primary-use case" for which the instruments were originally developed, he said.

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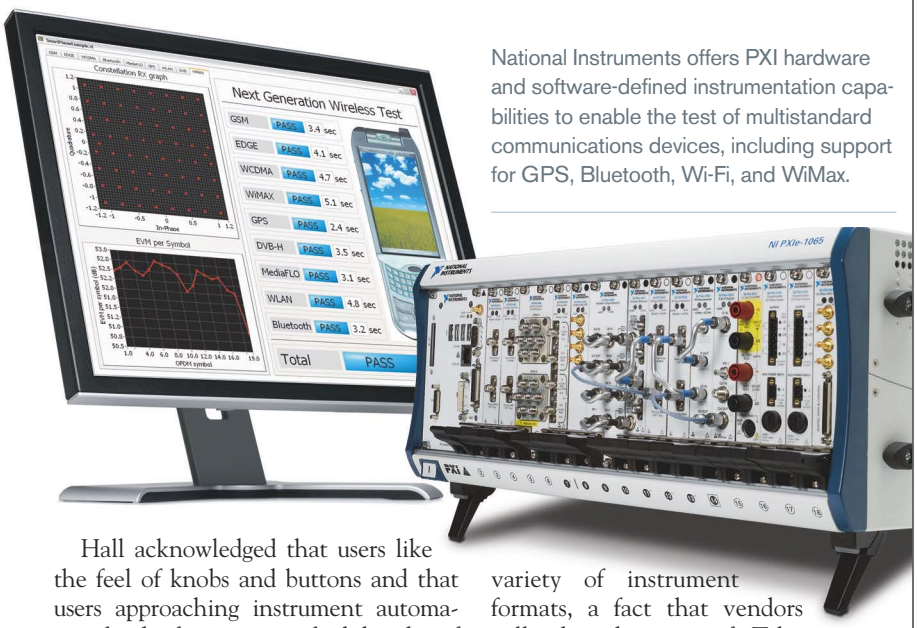

National Instruments offers PXI hardware and software-defined instrumentation capabilities to enable the test of multistandard communications devices, including support for GPS, Bluetooth, Wi-Fi, and WiMax.

Hall acknowledged that users like the feel of knobs and buttons and that users approaching instrument automation for the first time can find the idea of programming scary. He studied computer engineering in college and still finds the task of programming an instrument in C somewhat difficult. The graphical LabView language, he said, simplifies the task, and the company provides many sample programs to help new users get started.

Christopher Ziomek, president of ZTec Instruments, which makes digitizers in formats including PXI and LXI, said his inclination as an engineer would be to grab a Tektronix scope if he wanted to make a measurement in a lab. He noted some practical considerations. For example, if you want to make measurements while power-cycling a PXI scope under test, you'd need two PXI chassis: one for the scope under test and one for the test equipment. "I'm more comfortable with something that has knobs," he said, even though ZTec has developed its Zscope software, which mimics a traditional oscilloscope's front panel on a computer screen.

ZTec's younger engineers are more comfortable with the modular format, Ziomek added, and are happy running Zscope on tablet PCs. Modular instruments can also enhance productivity. Given PXI or LXI instruments and a computer interface, engineers are more likely to automate a measurement that they would otherwise manually repeat many times if restricted to a traditional bench-top instrument.

Ultimately, there will be room for a variety of instrument formats, a fact that vendors will take advantage of. Tektronix, for example, maker of the traditional engineering scope that Ziomek favors for lab work, said at NIWeek that it was teaming up with National Instruments to develop a 10G-sample/sec, 3-GHz PXI digitizer. Craig Overhage, chief technology officer of Tektronix, said that the company had been looking at how to bring its high-bandwidth, high-sampling-rate oscilloscope technology to customers who prefer a modular-instrument architecture. Overhage said he sees different use cases for PXI scopes and traditional scopes, and he doesn't expect the introduction of the new PXI scope, which NI will market, to affect sales of the company's popular traditional instruments. **EDN**

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1 Nelson, Rick, "LXI speeds gigahertz measurements," *Test & Measurement World*, November 2007, pg 49, www.tmworld.com/article/322745-LXI_speeds_gigahertz_measurements.php.
2 "Prototyping Complex Communications Systems," National Instruments, NIWeek video, Aug 12, 2009, http://zone.ni.com/wv/app/doc/p/id/wv-1696.

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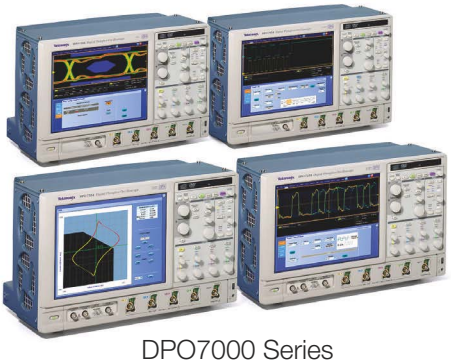

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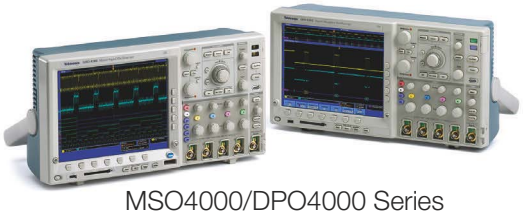

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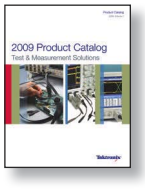

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PCB-layout techniques for gigasample ADCs

WHEN A MULTILAYER BOARD OPERATES AT SPEEDS GREATER THAN A FEW HUNDRED MEGAHERTZ, IT'S A CHALLENGE TO MAINTAIN SIGNALS WITHOUT MISMATCHES, LOSSES, DISTORTION, OR EMI. FOLLOW THESE GUIDELINES FOR PCB LAYOUT TO PRESERVE SIGNAL INTEGRITY AND ACHIEVE HIGH-SPEED PERFORMANCE.

As a general rule, when a design's speed rises to more than a few hundred megahertz, it requires a PCB (printed-circuit board) with four or more layers. The only exception occurs when the design uses small boards; in that case, a two-layer board may be acceptable. Developers typically perform these designs on evaluation boards for baluns, chip capacitors, resistors, and other small components.

Any board using a BGA (ball-grid array) with hundreds of pins can use no fewer than eight layers and typically uses more than 10 layers. The number of pins on the package of the largest chip on the board often determines the number of layers on a board. For example, National Semiconductor's (www.national.com) ADC10D1000 reference board comes in a 300-pin BGA package; the Xilinx (www.xilinx.com) Virtex-4 FPGA on the board is a 668-pin BGA. This arrangement requires at least an eight-layer board for a designer to gain access to all the pins. Given this constraint, you must also explore what other advantages the situation brings to the board design. It is no accident that you can achieve 10-bit performance with a 3-GHz sample rate on a board having multiple microwave signals, high-speed FPGAs, switching power supplies, and low-noise analog lines.

Nelco NP4000-6 epoxy from Park Electrochemical Corp (www.parkelectro.com) is a good material choice for designs requiring low loss and high durability. This material has a similar dielectric constant to that of conventional FR (fire-retardant)-4 board material, but Nelco 4000 provides better high-frequency performance. Another advantage of Nelco 4000 material is that you can use it for all layers, not just the top and bottom layers as with other microwave-PCB dielectrics, such as Teflon. The ADC10D1000 uses a 10-layer board. National Semiconductor also fabricated an identical board in FR-4 material, and, in some ways, this approach is better if the application can tolerate signal losses. Because of the higher loss tangent of FR-4, matching is less critical, providing for a better S_{11} reflection coefficient because FR-4 absorbs much of the signal that would cause reflections in the transmission line. However, lines in these designs should be no longer than 3 in. The difference between Nelco and FR-4 is negligible for the digital interface to the FPGA because the frequencies are lower than 2 GHz.

DDi Silicon Valley Division — **Pre-Release Stackup Report** — Pre-Release #: P22798A

Cust: DDI - Milpitas — Total Layers: 10

Part #: NATIONAL SEMI 10 LAYERS — Rev -

Finished Thickness: 0.0620 +/- 0.0060 — Finished Over: All

Lam Thickness: 0.0580 +/- 0.0030 — Material Type: NP 4000-6

Impedance Requirements:

L#	Impedance Type	Orig Line	Fin. Line	Ref Pln	2nd Ref Pln	Targeted Desired Impedance	Impedance Tolerance	Actual Calculated Impedance	Diff Line Centers	Diff Line Space	Original Coplanar Spacing	Finished Coplanar Spacing
1	DIF-Coated Microstrip Edg Cpld		.00325	2		100.00 Ω	+/- 10%	101.23 Ω	.01000	.00675		
1	SE-Coated Microstrip		.00425	2		50.00 Ω	+/- 10%	49.64 Ω				
3	DIF-Stripline Edg Cpld		.00400	2	4	100.00 Ω	+/- 10%	100.87 Ω	.00800	.00400		
3	SE-Stripline		.00600	2	4	52.00 Ω	+/- 10%	51.30 Ω				
6	DIF-Stripline Edg Cpld		.00400	7	5	100.00 Ω	+/- 10%	100.87 Ω	.00800	.00400		
6	SE-Stripline		.00600	7	5	52.00 Ω	+/- 10%	51.30 Ω				
8	DIF-Stripline Edg Cpld		.00400	9	7	100.00 Ω	+/- 10%	100.87 Ω	.00800	.00400		
8	SE-Stripline		.00600	9	7	52.00 Ω	+/- 10%	51.30 Ω				
10	DIF-Coated Microstrip Edg Cpld		.00325	9		100.00 Ω	+/- 10%	101.23 Ω	.01000	.00675		
10	SE-Coated Microstrip		.00425	9		50.00 Ω	+/- 10%	49.64 Ω				

Controlled Impedance Notes:

Lamination Stackup:

L#/Type	Description:	Thickness and Tolerances: Cu+:	Laminate/PrePreg:		Base Material Rqmts: Type: Description:	Dk @ 1Ghz
1 Sig	Foil (H oz)	.00060				
	Pre-Preg (1 x 1080)		.0027	+/- 0.0003	NP 4000-6	3.9
2 Pln	Core 0.0060 1/H	.00120	.0060		NP 4000-6	
3 Sig		.00060				4.1
	Pre-Preg (1 x 2113)		.0080	+/- 0.0008	NP 4000-6	4.18
	Pre-Preg (1 x 2116)					
4 Pln	Core 0.0030 1/1	.00120	.0030		NP 4000-6	
5 Pln		.00120				4.35
	Pre-Preg (1 x 2116)		.0080	+/- 0.0008	NP 4000-6	4.18
	Pre-Preg (1 x 2113)					
6 Sig	Core 0.0060 H/1	.00060	.0060		NP 4000-6	
7 Pln		.00120				4.1
	Pre-Preg (1 x 2116)		.0080	+/- 0.0008	NP 4000-6	4.18
	Pre-Preg (1 x 2113)					
8 Sig	Core 0.0060 H/1	.00060	.0060		NP 4000-6	
9 Pln		.00120				4.1
	Pre-Preg (1 x 1080)		.0027	+/- 0.0003	NP 4000-6	3.9
10 Sig	Foil (H oz)	.00060				

Target Post-Lam Thickness: 0.0580 +/- 0.0030

Copper Oz Legend: H=1/2oz T=3/8oz Q=1/4oz E=1/8oz S=1/16oz

Stackup Notes:

***Laser drilled microvias 1-2

PLEASE RETURN APPROVED STACK-UP TO DDI WITH DATA SET PRIOR TO MANUFACTURING

Figure 1 This stackup report gives the dimensions for matched impedance for both surface (microstrip) and embedded (stripline) transmission lines (courtesy DDI).

Before beginning any layout, you must obtain the stackup data from the PCB manufacturer because the data gives the dimensions for matched impedance for both surface (microstrip) and embedded (stripline) transmission lines. **Figure 1** shows stackup data from DDI (www.ddiglobal.com). Other manufacturers offer similar data. Matched lines are critical for high-frequency signals. Ideally, you want coaxial cable, but this choice is not economical except for the most critical applications, such as military, high-end commercial, or aerospace equipment. The cost is typically prohibitive in consumer applications, so with multilayer PCBs, stripline or microstrip rather than expensive miniature coaxial cable is your best option.

Impedance is constant in coaxial cable because the surrounding ground shield is at a constant distance from the center conductor. This situation translates to a constant velocity factor and thus uniform speed of the wave traveling inside the coaxial cable. The coaxial cable presents the best impedance match to a signal. If multiple signal lines are close together on a PCB with limited space, you should use ultrathin coaxial cables, such as 50Ω SRC023, with an outside diameter of 23 mils, for high-performance transmission and isolation. You layer this coaxial cable on the surface of the PCB. Again, using this cable for consumer applications is cost-prohibitive, and this technique finds use primarily in satellite and military applications in which dozens of high-frequency signals must transmit in a small space.

If using coaxial cable is impractical, one possible choice is the use of a microstrip (**Reference 1**). The basic principle of this technique is that you use the horizontal trace contributing to the inductance and the trace above the ground plane to calculate the square root of the inductance divided by the capacitance. A given width for a given thickness yields an impedance. In coaxial cable, the wave travels with 100% uniform surroundings; the outer-shield conductor is at a constant distance from the center conductor. You cannot duplicate this topology on a PCB microstrip.

Microstrip improves on using just a "random" trace but is far from ideal. Even if you precisely calculate the trace width and precisely consider the trace's height from the ground plane, it does not even approach a perfect match. The intuitive explanation, without introducing Maxwell's field equations, is that the dielectric below the trace is thicker than air. The dielectric above the trace is air. Take, for example, FR-4, with a dielectric constant of approximately four. The wave traveling in the dielectric travels at approximately half the speed of that in air. Thus, microstrips cannot work over long distances. The signal above the trace travels at twice the speed of that in the dielectric. However, sometimes you have no other choice; for runs of less than a quarter-wavelength, using microstrip is a viable alternative. For long runs, the mismatch dominates, so you cannot use microstrip. There are times when you cannot avoid using microstrip, such as when you must connect an SMA connector, when your design requires surface test points, or when the design has only a two-layer PCB.

Another improvement is the use of balanced differential lines over the ground plane. Two lines have equal and opposite currents, ideally canceling the external field. This cancellation makes this type of transmission line less dependent on the ground planes than a single-conductor microstrip would be. However, the differential lines lack the enclosure of coaxial cable. In a differential microstrip, the ground plane is only partially responsible for the matching (**Figure 2**). Most of the matching depends on the conjugate line. This technique is still vulnerable to both radiating and receiving interference

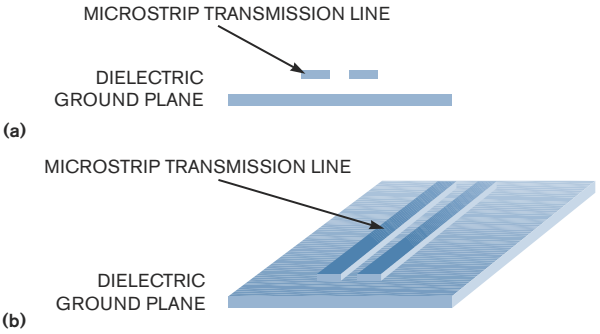

Figure 2 In a side view (a) and a perspective view (b) of the differential microstrip line, the ground plane is only partially responsible for the matching. Most of the matching depends on the conjugate line.

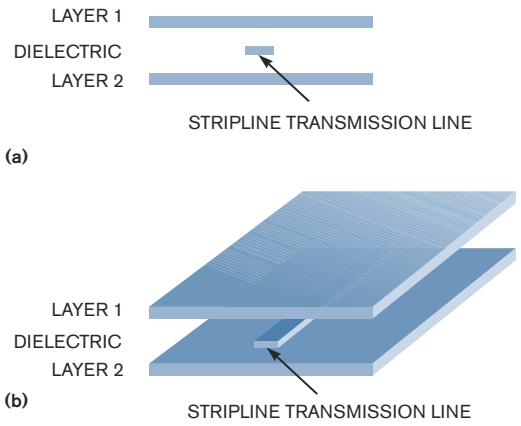

Figure 3 Conventional single-ended stripline in a side view (a) and a perspective view (b), although an improvement over microstrip, is still not ideal.

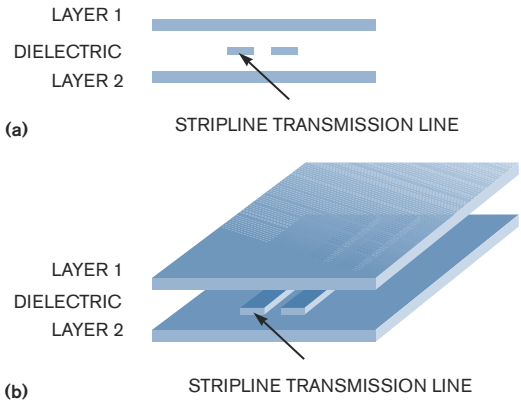

Figure 4 Differential stripline offers good matching and excellent EMI shielding in both a side view (a) and a perspective view (b).

signals. On a two-layer PCB, it is the best choice other than using rigid coaxial cable. It does require almost twice as much area, however.

The solution to the microstrip issue is to use striplines sandwiched between two planes (**Figure 3**). This approach allows for a uniform dielectric around the transmission line. However, it still does not provide uniform return ground for the conductor. It does not have coaxial cable's major advantage—that the ground shield surrounds the signal line by 360°. In the case of the stripline, only the top and bottom provide for the ground return. Another advantage of using striplines is that they have shielding from the outside world, preventing not only interference but also unnecessary radiating signals. The match, although better, does not rival the performance of coaxial cable. As in the case of microstrip, differential lines improve performance at the expense of occupying more space (**Figure 4**).

The ADC10D1000 uses impedance-matched differential stripline with equal and opposite currents on each line. The matching depends on the thickness of the dielectric, the dielectric constant of the material, and the spacing and thickness of the balanced line. You obtain all of this information from the PCB manufacturer. Using this approach and embedding the stripline between two power-supply or ground planes makes the EMI (electromagnetic interference) too small to measure.

The entire system on the ADC-10D1000 reference board is fully differential, taking advantage of not only the chip's CMR (common-mode rejection) but also the matching of impedances from the outside world to the input of the chip. The drawback of this approach is that it almost doubles complexity. The thermal noise increases in quadrature due to the increase in total active components, and power consumption increases accordingly. You would be lucky to retrieve even 6 bits in a 1G-sample, single-ended architecture.

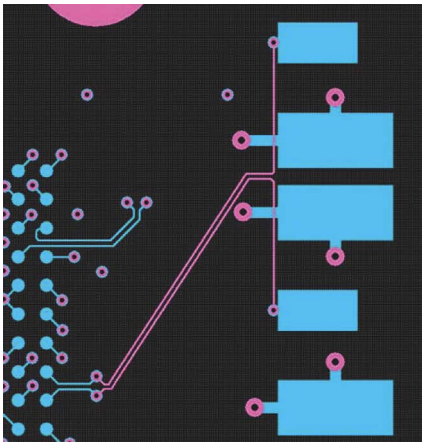

Figure 5 You must immediately bring together the positive and negative input-voltage signals to conform to the 100Ω balanced transmission line.

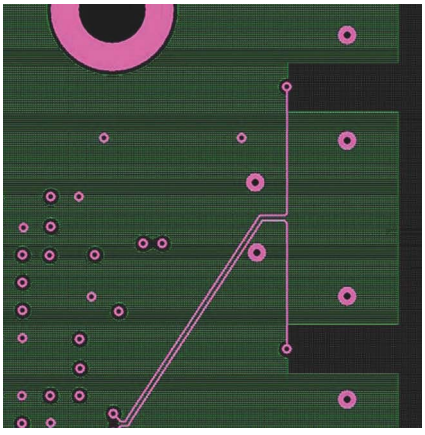

Figure 6 The general rule is to keep the balanced transmission line intact as long as possible to maintain matching. You must remove the green ground layer underneath the SMA landing pad, Layer 2, because it would form a large capacitor with the landing pad. This board has no conducting material under the SMA landing pad until Layer 7. Layer 7 must be an ac ground for proper impedance matching.

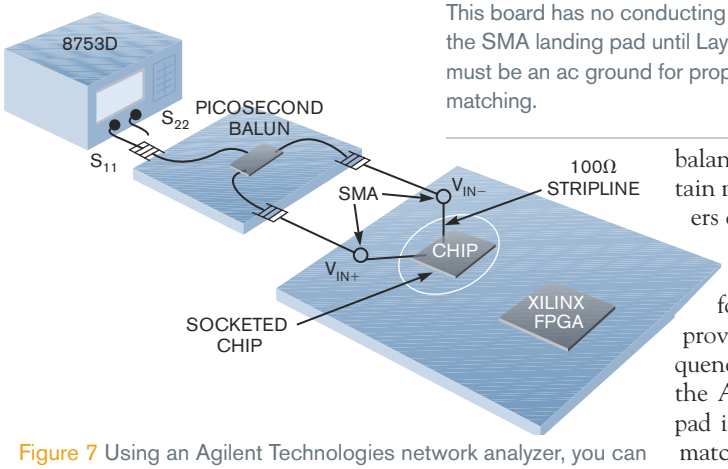

Figure 7 Using an Agilent Technologies network analyzer, you can achieve better than −10-dB return loss at frequencies as high as 3 GHz.

Early in the design cycle of the ADC-10D1000, its designers determined that the input interface would be as simple as possible, placing any baluns, amplifiers, and relays outside the board. They also used no relays or unnecessary traces because all these components would degrade the performance of the board. The following general approach achieves good matching and provides for the broadest bandwidth with minimal EMI. From the input pins of the ADC, immediately place vias and move down at least one layer for the transmission line. In the case of the ADC10D1000, designers chose Layer 3 as the transmission line. This layer forms the heart of the stripline transmission line, with layers 2 and 4 as the ac ground, shielding the signal from outside interference. Because it is a balanced stripline, it maintains its impedance for longer distances than does an open, single-trace, unbalanced surface transmission line.

You must immediately bring together the positive and negative input-voltage signals to conform to the 100Ω balanced transmission line (**Figure 5**). This step is critical for good performance. At the SMA-connector end, the via comes back up to the surface layer. The general rule is to keep the balanced transmission line intact as long as possible to maintain matching (**Figure 6**). Another major rule, which designers often overlook, is the impedance matching of the SMA connector to the PCB. Although the SMA connector itself is matched to 50Ω, the landing pad on the PCB for the SMA connector is not. Unless you make special provisions, the performance of the board deteriorates at frequencies greater than 1 GHz. With the SMA connectors that the ADC10D1000 reference design uses, the SMA landing pad is about four times wider than a 50Ω trace. For a 50Ω match, the associated ground plane is Layer 7. You must remove the metal on layers 2 through 6.

Using these layout rules, you can achieve superb broadband matching. Using an Agilent Technologies (www.agilent.com)

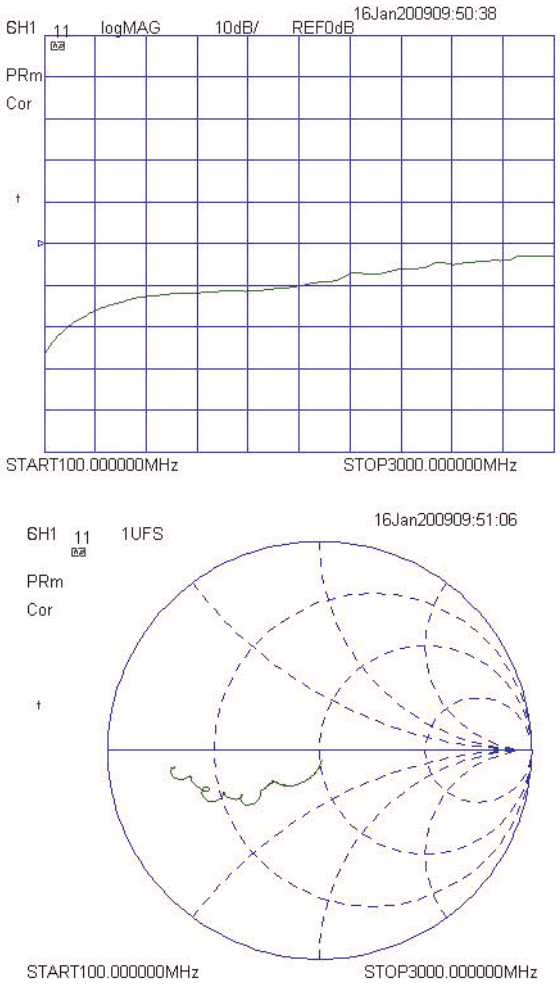

Figure 8 The S_{11} of the input match with a 100Ω termination resistor without removing layers 2 through 6 works at frequencies as high as 1.5 GHz.

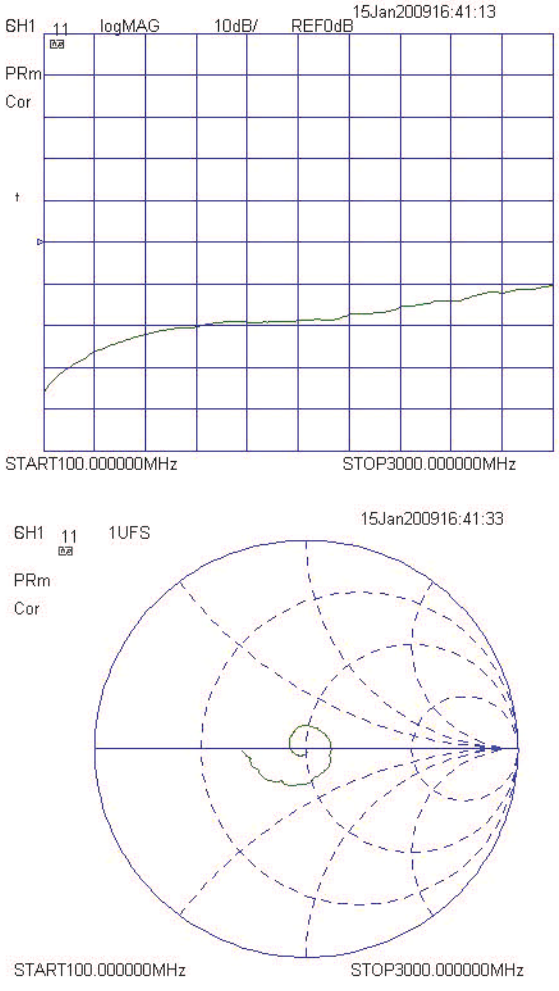

Figure 9 With layers 2 through 6 blank under the SMA landing pad, this layout is a dramatic improvement and is usable at frequencies as high as 3 GHz.

8753D network analyzer, you can achieve better than −10-dB return loss at frequencies as high as 3 GHz (**Figure 7**). **Figure 8** shows the S_{11} of the input match with a 100Ω termination resistor without removing layers 2 through 6. The matching works at frequencies as high as 1.5 GHz. **Figure 9** shows the same layout with the removal of layers 2 through 6. It is a dramatic improvement and is usable at frequencies as high as 3 GHz. **Figure 10** shows the input match with the ADC10D1000 in place. The worst-case return loss is better than −12 dB at 100 MHz to 3 GHz.

The exact amount of ground plane to remove from layers 2 through 6 is a subject of debate. Layers 2 through 6 contribute to the impedance of the landing pad even if you remove them. Not all of the fields from the SMA landing pad terminate on Layer 7; some terminate on layers 2 through 6. A 2-D field-solver program can solve many of the details and determine clearance. If a field-solver program is unavailable, you can get this data for SMA landing pads from any reputable PCB vendor. The vendor should be able to provide this information for the exact dimensions for its process. If neither of these options is available, clear each layer—layers 2 through 6, for example—by three to five widths of the stripline conductor (**Figure 11**).EDN

REFERENCE

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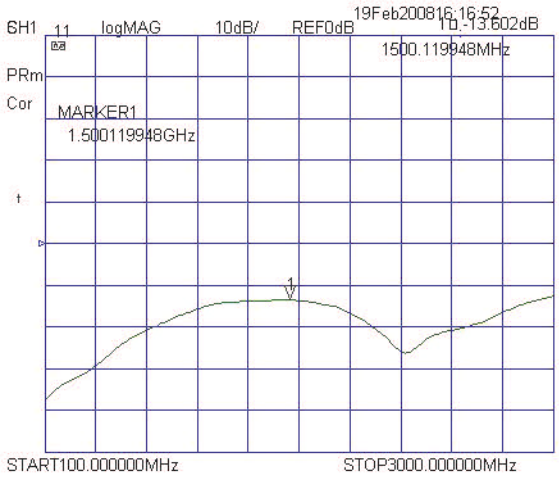
AUTHOR'S BIOGRAPHY

Edison Fong is an instructor at the University of California—Berkeley Extension School, where he teaches courses in radio frequency and acts as a consultant on chip design and board-level design. Previously, he worked at National Semiconductor. He holds nine patents and has published more than 30 papers. Fong received bachelor's and master's degrees in electrical engineering from the University of California—Berkeley, a degree in engineering science from the University of Santa Clara (Santa Clara, CA), and a doctorate from the University of San Francisco. His personal interests include ham radio, photography, bicycling, and jogging.



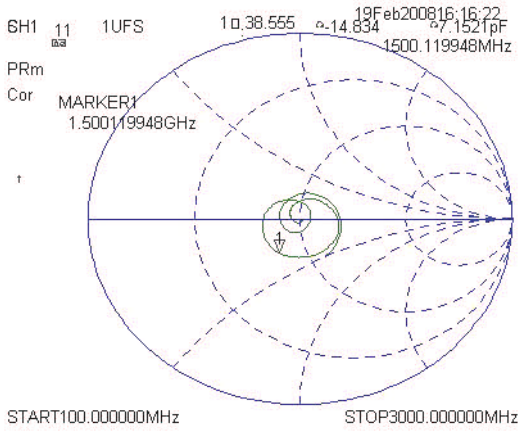


Figure 10 With the ADC10D1000 in place, the worst-case return loss is better than −12 dB at 100 MHz to 3 GHz.

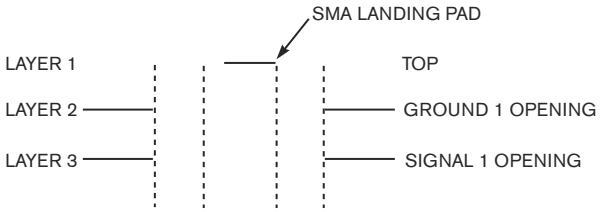
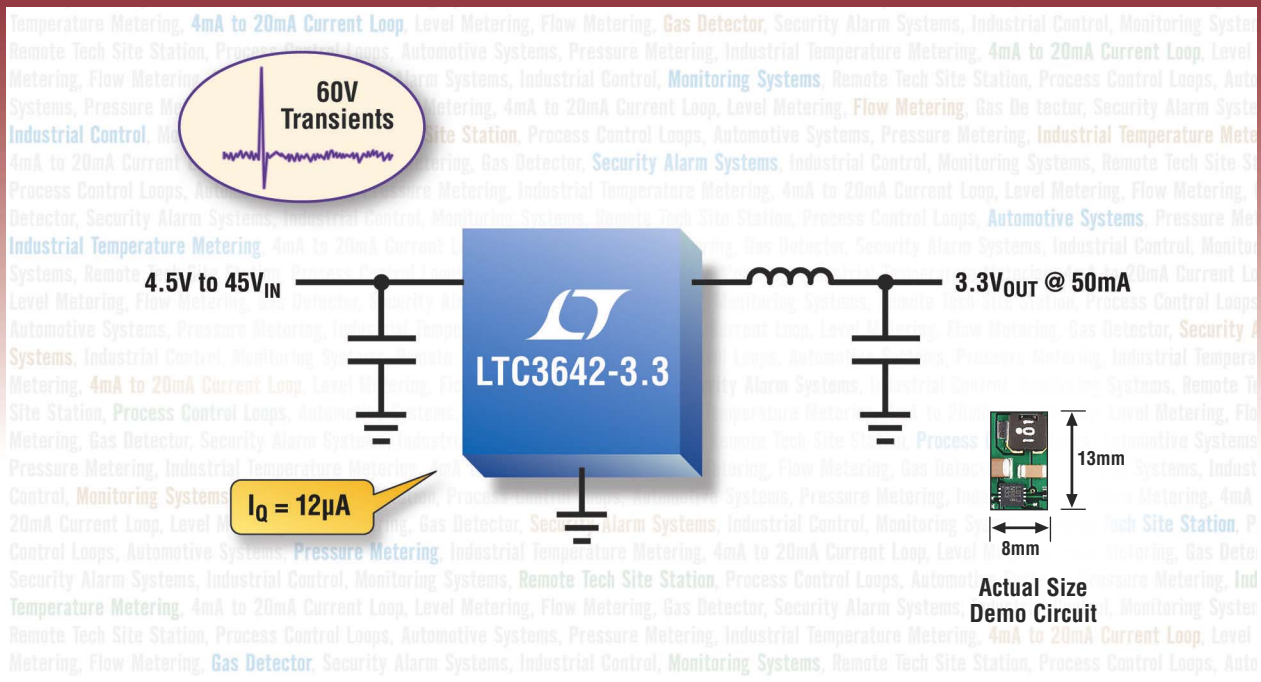


Figure 11 The exact amount of ground plane to remove from layers 2 through 6 is a subject of debate. If a field-solver program or data from the PCB vendor is unavailable, clear each layer with three to five widths of the stripline conductor.

45V Synchronous Buck



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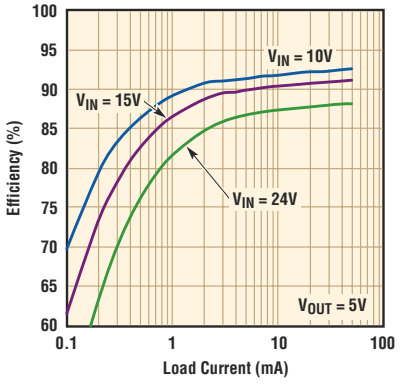

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READERS SOLVE DESIGN PROBLEMS

Negative-to-negative switch-mode converter offers high current and high efficiency

Budge Ing, Maxim Integrated Products Inc, Sunnyvale, CA

When converting a negative-output power supply to one with less-negative output, you must ensure that variations in input voltage don't affect the output voltage. All such supplies include an internal reference voltage that enables output-voltage regulation. You usually refer this reference to the most negative rail, which is ground. Thus, the output voltage of such a converter depends on the accuracy of its negative input supply voltage. The circuit in **Figure 1** lacks that limitation. Delivering output currents as high as 4A with efficiencies better than 90%, it generates a negative output with the help of an op amp and a switch-mode boost converter. Closed-loop feedback regulates the output voltage with respect to ground, the most positive rail,

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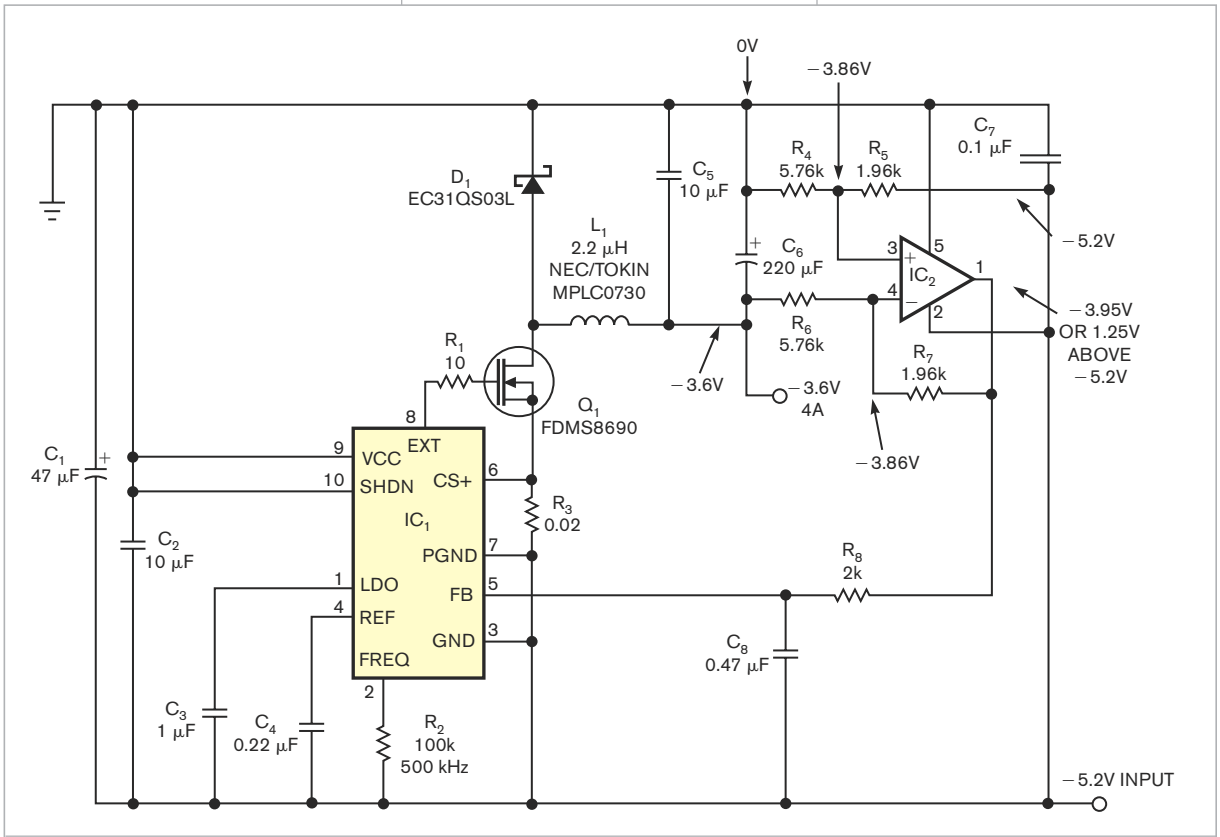

Figure 1 A switch-mode converter generates a regulated negative supply voltage from a more-negative input voltage.

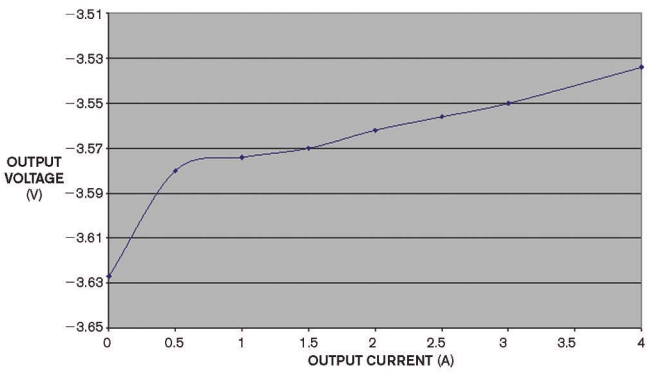

Figure 2 Output voltage for the circuit in Figure 1 varies with output current.

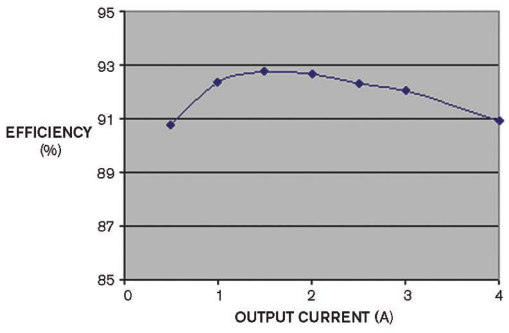

Figure 3 Conversion efficiency for the circuit in Figure 1 varies with output current.

which is also the node from which current is delivered to the load.

The circuit converts a −5.2V supply voltage to −3.6V. The boost converter, IC_1, regulates its output voltage to maintain its feedback voltage at −3.95V—1.25V above −5.2V. Resistor R_8 and capacitor C_8 form a low-pass filter that stabilizes the voltage at FB. You must then select the R_4/R_6 and R_5/R_7 pairs to produce the desired output voltage. Making R_4 and R_5 equal and making R_6 and R_7 equal improves the common-mode performance. The ratio of R_4 to R_5 determines the voltage level at the positive input of op amp IC_2, whose closed-loop configuration ensures that the same voltage appears at its negative input. Knowing IC_2's output voltage, −3.95V, and its negative input voltage lets you determine the output voltage using the values of R_6 and R_7: $V_{OUT}=-V_{REF}(R_6/R_7)$, where V_{REF} is the 1.25V nominal reference voltage of IC_1, $R_4=R_6$, and $R_5=R_7$.

The component values in **Figure 1**—for example, 1.96 kΩ for R_5 and R_7 and 5.76 kΩ for R_4 and R_6—produce an output voltage of −3.76V. Graphs of output voltage versus output current (**Figure 2**) and efficiency versus output current (**Figure 3**) illustrate this circuit's performance. EDN

ADC for programmable logic uses one capacitor

Jef Thoné and Robert Puers,
Katholieke Universiteit Leuven, Leuven, Belgium

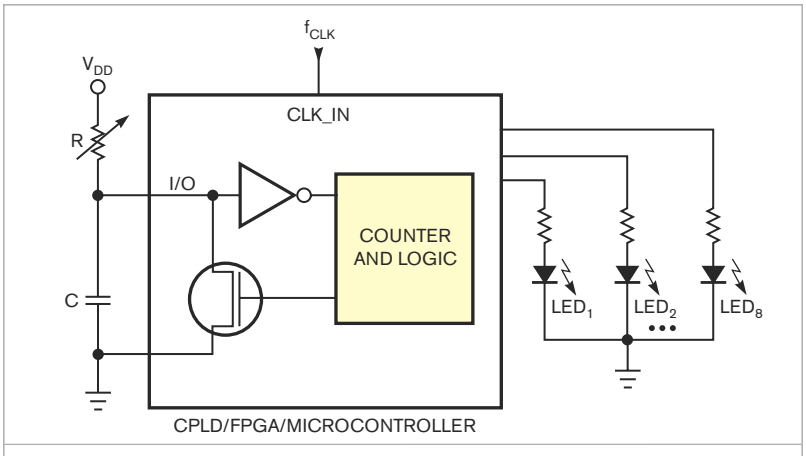

Figure 1 This circuit charges a capacitor through a resistor while measuring the time to charge the capacitor to a certain voltage.

Many electronic devices require user input for setting the application properties. Typical input devices include pushbuttons, potentiometers, and touchscreens. To minimize overall project cost, you may have to select low-range microcontrollers, FPGAs (field-programmable gate arrays), or PLDs (programmable-logic devices). These devices don't provide a wide range of peripherals and often lack analog-to-digital-conversion capability, which can prove annoying when trying to acquire user input. This Design Idea describes a method for adding a low-end ADC to a single programmable-logic I/O pin. The circuit charges a capacitor through a resistor while measuring the time to charge the capacitor to a certain voltage.

Before each measurement, the capacitor discharges to 0V. A single I/O pin can perform both the dis-

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DMM	Digits	DC Accuracy	Max Readings	Function/Range Changes	IO
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34410A	6 ½	0.0030%	10,000 / sec	2.6 ms	GPIB, USB, LAN (LXI)
34411A/ L4411A	6 ½	0.0030%	50,000 / sec	2.6 ms	GPIB, USB, LAN (LXI)
34420A	7 ½	0.0030%	250 / sec	.02 sec	GPIB, RS-232
3458A	8 ½	0.0008%	100,000 / sec	3.0 ms	GPIB

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charging and the timing. For an FPGA or a PLD, you can perform a discharge by setting the I/O as an output pin and forcing a zero at that pin. You can charge the capacitor by setting the I/O as an input pin, which gives it a high impedance. The capacitor charges through the potentiometer (**Figure 1**). Meanwhile, a counter starts, and the CPLD monitors the input voltage. As soon as the capacitor voltage reaches the threshold, the counter stops at a value that is a measure of the charging time. The charging time or counter value relates to the clock frequency, the value of the resistor, the value of the capacitor, and the input threshold voltage:

$$V_{TH} = V_{DD} \times \left(1 - e^{\frac{-t}{R \times C}}\right)$$

$$T = \frac{COUNTERVALUE}{f_{CLK}}$$

$$COUNTERVALUE = -f_{CLK} \times R \times C \times \ln\left(1 - \frac{V_{TH}}{V_{DD}}\right).$$

If you assume that the capacitor value, the input threshold voltage, and the clock frequency remain fairly constant over the operating range, the charging time is linearly dependent on the value of the resistor. If you replace the resistor with a potentiometer, a counter value depends on the potentiometer position. The application uses a Xilinx (www.xilinx.com) XC9500 XL CPLD (**Figure 2**). The I/O, which VHDL (very-high-speed-IC hardware-description language) declares as a tristate buffer, first shorts the capacitor. Hardware limits the output short-circuit current of the I/O pins to ±10 mA, so the capacitor's shorting should last long enough to guarantee a full discharge. You can calculate the minimum shorting time using the capacitor value, short-circuit current, and discharge voltage, assuming that the threshold voltage must discharge from the capacitor:

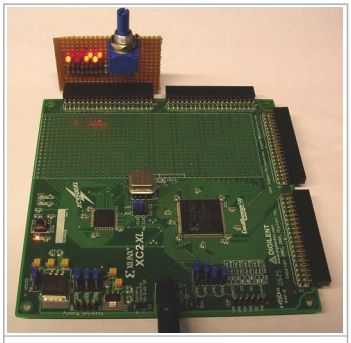

Figure 2 The application uses a Xilinx XC9500 XL CPLD.

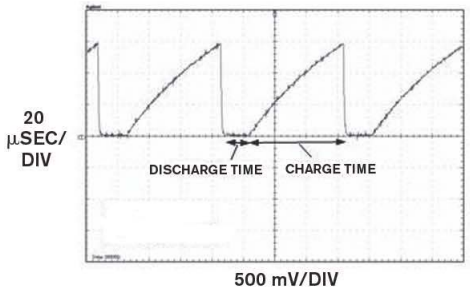

Figure 3 In this application, a 10-kΩ potentiometer in series with a 1-kΩ resistor charges a 22-nF capacitor.

$$t_{DISCMIN} = V_{THRESHOLD} \times \frac{C}{I_{SHORT}}.$$

The discharge delay can be realized with a small counter. After the discharge time, the I/O pin acts as an input, which causes the capacitor to charge through a pullup potentiometer. Meanwhile, the internal counter starts. When the capacitor voltage reaches the input threshold voltage, the counter stops. Eight LEDs show the 8-bit value. In this application, a 10-kΩ potentiometer in series with a 1-kΩ resistor charges a 22-nF capacitor. The input clock of the PLD is 1.8432 MHz. The input threshold is 1.5V at a supply of 3.3V. This arrangement allows a measurement range between a counter value of 25 and 270, equivalent to a resolution of almost 8 bits. **Figure 3** shows the capacitor charging/discharging waveform.

Every IC's I/O pin has a certain bias sink or source current, causing a voltage drop over the charging resistor. This situation limits the charge voltage to $V_{DD} - R_{CHARGE} \times I_{BIAS}$. In other words, if the charging resistance is too large, the capacitor doesn't charge above the input-pin threshold voltage, stopping the circuit's operation. Similar applications for microcontrollers or PLDs (**references 1** through **5**) include adding multiple inputs to a single I/O pin and using a different pullup-resistor value for each input. By discriminating the charging times for each resistor, the PLD can decide which resistor or combination of resistors the user has actuated.

Another application for microcontrollers is temperature measurement. By replacing the pullup resistor with a PTC (positive-temperature-coefficient) or an NTC (negative-temperature-coefficient) resistor, you can derive the temperature from the charging time after calibration. You can also use these devices to make true analog-to-digital measurements. By replacing the pullup resistor with a voltage-controlled current source, an input-voltage change causes a linear change in the charging time, providing a real analog-to-digital conversion. EDN

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LINEAR TECHNOLOGY

DESIGN NOTES

Battery Conditioner Extends the Life of Li-Ion Batteries

Design Note 472

George H. Barbehenn

Introduction

Li-Ion batteries naturally age, with an expected lifetime of about three years. But, that life can be cut very short–to under a year–, if the batteries are mishandled. It turns out that the batteries are *typically* abused in applications where intelligent conditioning would otherwise significantly extend the battery lifetime. The LTC4099 battery charger and power manager contains an I²C controlled battery conditioner that maximizes battery operating life, while also optimizing battery run time and charging speed (see Figure 1).

The Underlying Aging Process in Li-Ion Batteries

Modern Li-Ion batteries are constructed of a graphite negative terminal, cobalt, manganese or iron phosphate positive terminal and an electrolyte that transports the lithium ions.

The electrolyte may be a gel, a polymer (Li-Ion/Polymer batteries) or a hybrid of a gel and a polymer. In practice, no suitable polymer has been found that transports lithium ions effectively at room temperature. Most 'pouch' Li-Ion/Polymer batteries are in fact hybrid batteries containing a combination of polymer and gel electrolytes.

The charge process involves lithium ions moving out of the negative terminal material, through the electrolyte and into the positive terminal material. Discharging is the reverse process. Both terminals either release or absorb lithium ions, depending on whether the battery is being charged or discharged.

The lithium ions do not bond with the terminals, but rather enter the terminals much like water enters a sponge; this process is call 'intercalation.' So, as is often the case with charge-based devices such as electrolytic capacitors, the resulting charge storage is a function of both the materials used and the physical structure of the material. In the case of the electrolytic capacitor, the foil is etched to increase its surface area. In the case of the Li-Ion battery the terminals must have a sponge-like physical makeup to accept the lithium ions.

The choice of positive terminal material (cobalt, manganese or iron phosphate) determines the capacity, safety and aging properties of the battery. In particular, cobalt provides superior capacity and aging characteristics, but it is relatively unsafe compared to the other materials. Metallic lithium is flammable and the cobalt positive terminal tends to form metallic lithium during the discharge process. If several safety measures fail or are defeated, the resulting metallic lithium can fuel a "vent with flame" event.

Consequently, most modern Li-Ion batteries use a manganese or iron phosphate-based positive terminal. The price for increased safety is slightly reduced capacity and increased aging.

Aging is caused by corrosion, usually oxidation, of the positive terminal by the electrolyte. This reduces both the effectiveness of the electrolyte in lithium-ion transport and the sponge-like lithium-ion absorption capability of

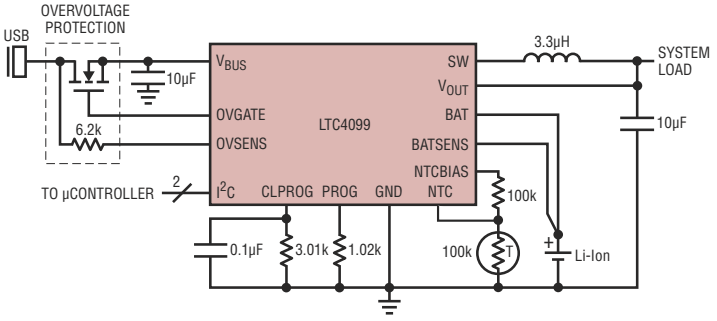

Figure 1. The LTC4099 with I²C Controlled Battery Conditioner

the positive terminal. Battery aging results an increase of the battery series resistance (BSR) and reduced capacity, as the positive terminal is progressively less able to absorb lithium ions.

The aging process begins from the moment the battery is manufactured and cannot be stopped. However, battery handling plays an important role in how quickly aging progresses.

Conditions that Affect the Aging Process

The corrosion of the positive terminal is a chemical process and this chemical process has an activation energy probability distribution function (PDF). The activation energy can come from heat or the terminal voltage. The more activation energy available from these two sources the greater the chemical reaction rate and the faster the aging.

Li-Ion batteries that are used in the automotive environment must last 10 to 15 years. So, suppliers of automotive Li-Ion batteries do not recommend charging the batteries above 3.8V. This does not allow the use of the full capacity of the battery, but is low enough on the activation energy PDF to keep corrosion to a minimum. The iron phosphate positive terminal has a shallower discharge curve, thus retaining more capacity at 3.8V.

Battery manufacturers typically store batteries at 15°C (59°F) and a 40% state of charge (SoC), to minimize aging. Ideally, storage would take place at 4% or 5% SoC, but it must never reach 0%, or the battery may be damaged. Typically, a battery pack protection IC prevents a battery from reaching 0% SoC. But pack protection cannot prevent self-discharge and the pack protection IC itself consumes some current. Although Li-Ion batteries have less self-discharge than most other secondary batteries, the storage time is somewhat open-ended. So, 40% SoC represents a compromise between minimizing aging and preventing damage while in storage (see Figure 2).

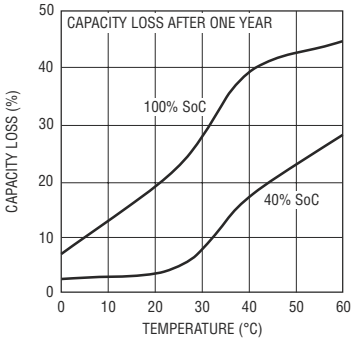

Figure 2. Yearly Capacity Loss vs Temperature and SoC for Li-Ion Batteries

In portable applications, the reduction in capacity from such a reduced SoC strategy is viewed negatively in marketing specifications. But it is sufficient to detect the combination of high ambient heat and high battery SoC to implement an algorithm that minimizes aging while ensuring maximum capacity availability to the user.

Battery Conditioner Avoids Conditions that Accelerate Aging

The LTC4099 has a built-in battery conditioner that can be enabled or disabled (default) via the I²C interface. If the battery conditioner is enabled and the LTC4099 detects that the battery temperature is higher than ~60°C, it gently discharges the battery to minimize the effects of aging. The LTC4099 NTC temperature measurement is always on and available to monitor the battery temperature. This circuit is a micropower circuit, drawing only 50nA while still providing full functionality.

The amount of current used to discharge the battery follows the curve shown in Figure 3, reaching zero when the battery terminal voltage is ~3.85V. If the temperature of the battery pack drops below ~40°C and a source of energy is available, the LTC4099 once again charges the battery. Thus, the battery is protected from the worst-case battery aging conditions.

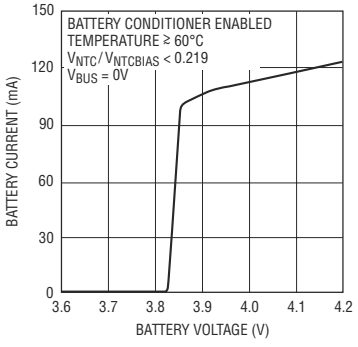

Figure 3. Battery Discharge Current vs Voltage for the LTC4099 Battery Conditioning Function

Conclusion

Although the aging of Li-Ion batteries cannot be stopped, the LTC4099's battery conditioner ensures maximum battery life by preventing the battery-killing conditions of simultaneous high voltage and high temperature. Further, the micropower, always on NTC monitoring circuit ensures that the battery is protected from life-threatening conditions at all times.

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Use two phases to cut current and improve EMI

Goran Perica, Linear Technology, Milpitas, CA

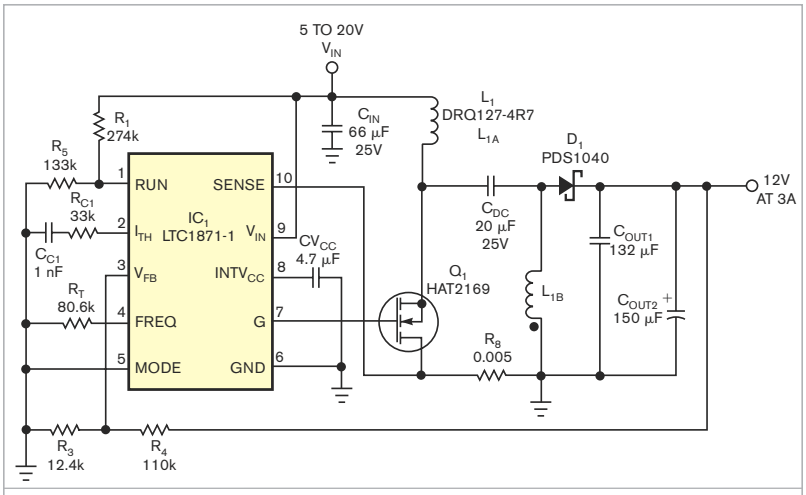

Figure 1 A single-phase SEPIC has low input ripple currents and is suitable for power levels of 5 to 50W.

In dc/dc-converter applications in which the input voltage may be lower or higher than the output voltage, you can use either a flyback converter or a SEPIC (single-ended-primary-inductor converter). SEPICs offer lower input-current ripple and higher efficiency than do flyback designs. Both converters suffer from relatively high output-current ripple, especially at high load currents and low input voltages. As output-current ripple increases, so does the circuit's output-filter-capacitance requirement, which increases size and cost. You can reduce output-current and -voltage ripple without increasing the application size and cost by using a multiphase SEPIC or flyback converter. Using a multiphase flyback circuit also greatly reduces the input-current ripple.

To evaluate the benefits of a dual-phase versus a single-phase SEPIC, this Design Idea compares two designs running at 300-kHz switching frequency. For consistency, both examples use the same power components, resulting in twice the output power in the two-phase design.

The single-phase SEPIC circuit can generate 3A of output current (**Figure 1**). SEPICs are typically 1 to 2% more efficient than flyback converters. **Figure 2** shows the output diode's current (bottom trace) at minimum input voltage and maximum load and the output-voltage ripple (top trace). The circuit's output capacitors must handle the peak output-diode current of 14A. Even though the circuit uses four low ESR (equivalent-series-resistance) output capacitors, output-voltage ripple is still 110 mV p-p. The aluminum output capacitor, C_{OUT2}, doesn't help much in reducing the output ripple due to its much higher ESR. C_{OUT2} mainly helps reduce load transients by adding bulk capacitance to the output rail.

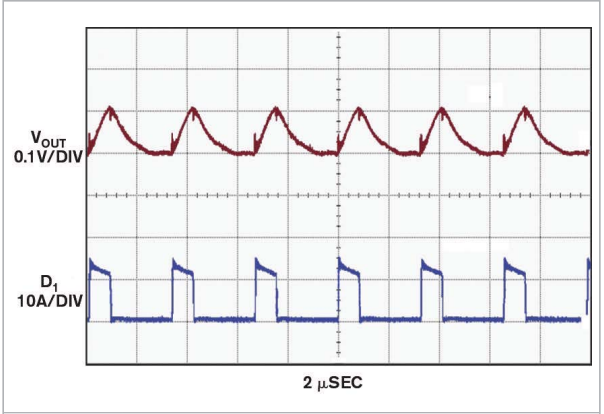

Figure 2 The single-phase circuit in Figure 1 has a peak capacitor output current of about 14A (bottom trace).

Figure 3 (pg 52) shows a two-phase converter, which is similar to the single-phase converter in **Figure 1** except for the addition of an identical second-phase power stage. The second phase halves the peak inductor, MOSFET, and output-diode currents. The 50% lower peak output-diode currents produce 50% lower output ripple (**Figure 4**, pg 52). Also, the output-ripple-current frequency doubles, thus making it easier to filter out with an additional LC filter if necessary.

The benefits of using a dual-phase converter become clear when you consider output-capacitor ripple current (**Figure 5**, pg 52). The two-phase converter's output-capacitor ripple current is always lower than that of an equivalent single-phase converter. Depending on the duty cycle, the two-phase converter's output-capacitor ripple current can approach 0A at a 50% duty cycle. Inductor ripple current is still present, and you can reduce it by using larger inductors.

Using a two-phase converter means that you can use smaller inductors, MOSFETs, output diodes, and output capacitors than you can use in an equivalent single-phase converter. Because high-power designs may need to use more than one MOSFET anyway, a dual-phase design may need only one additional smaller inductor and one smaller diode. Output LC filters can also be smaller because of the doubling of the output ripple frequency. Finally, the EMI performance of a dual-phase SEPIC should be better than that of a single-phase converter because of lower current slew rates and smaller current loops. EDN

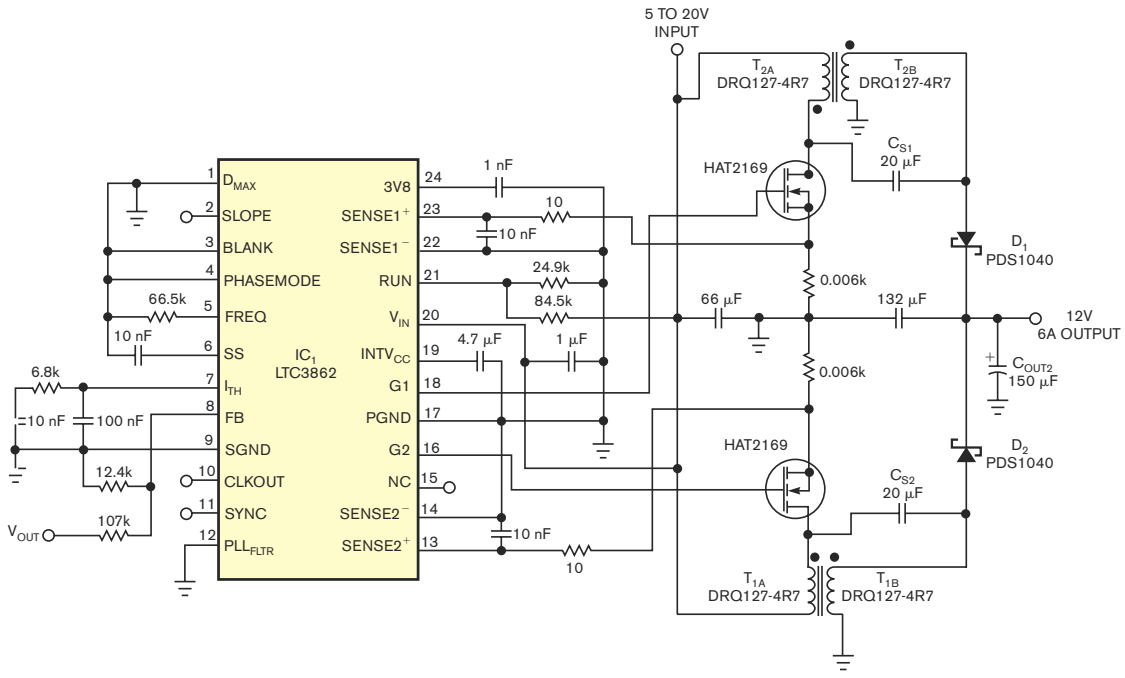

Figure 3 By adding second power stage and shifting the phase by 180°, you can reduce the output ripple currents by more than 50%.

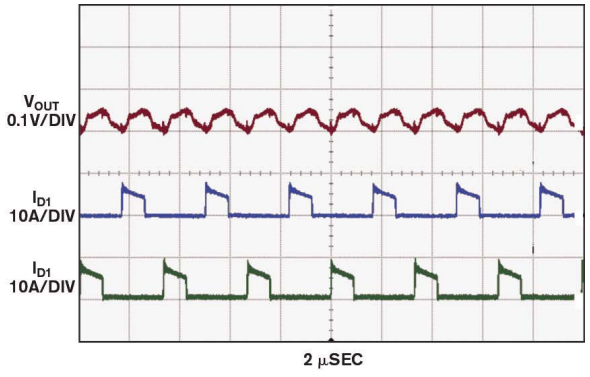

Figure 4 The output ripple current is 50% lower for a two-phase SEPIC. The output ripple voltage is 50% lower than that of a single-phase design with the same output capacitors.

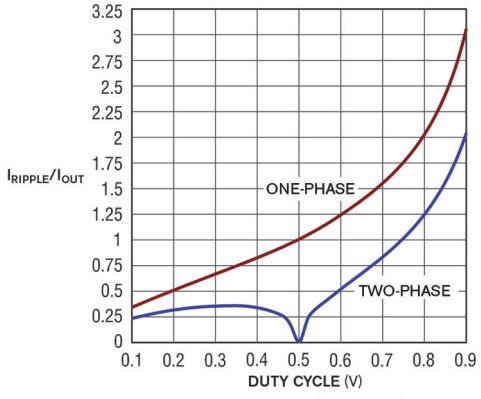

Figure 5 The normalized output-capacitor ripple current for single- and dual-phase SEPICs shows lower output ripple with a two-phase design.

Fader switch uses inexpensive controller

William Grill, Lenexa, KS

Customizing a model or a simulator with a bit of illumination is a nice touch. Rather than a simple on or off, you can add a touch of both refinement and control to your display with fading light. Employing a Microchip (www.microchip.com) 10F20x microcontroller, the circuit in **Figure 1** provides dual-rate fader control for a push-on/push-off switch, a momentary pushbutton switch, or a simple on/off SPST (single-pole/single-throw) switch. The circuit monitors and debounces the switch and generates a multiple-cycle, 470-Hz, PWM (pulse-width-modulated) output to drive LEDs or incandescent lamps. The circuit includes a MAX16823 (www.maxim-ic.com) IC that drives multiple LEDs.

The microcontroller produces 64 linear steps of a PWM signal between 0 and 100% duty cycle. The controller maintains each pulse width for a variable number of cycles employing a table in the assembly code (**Listing 1**,

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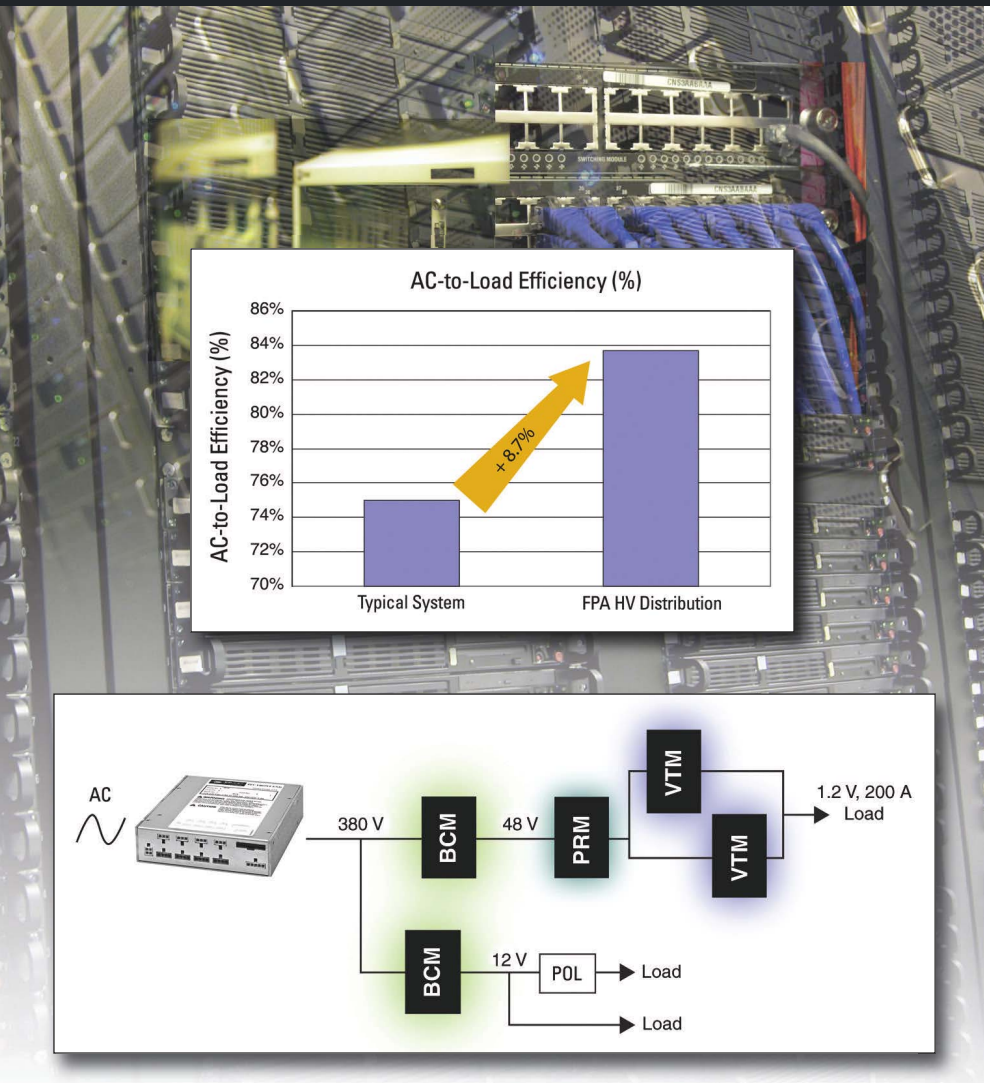

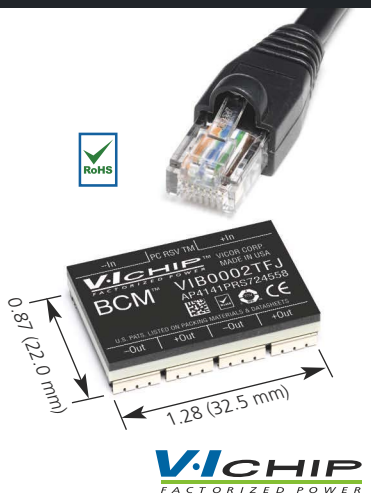

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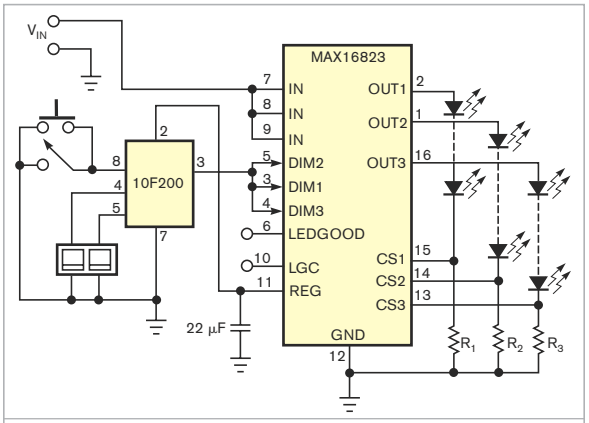

Figure 1 A microcontroller provides pulses with adjustable widths to create fading in LEDs.

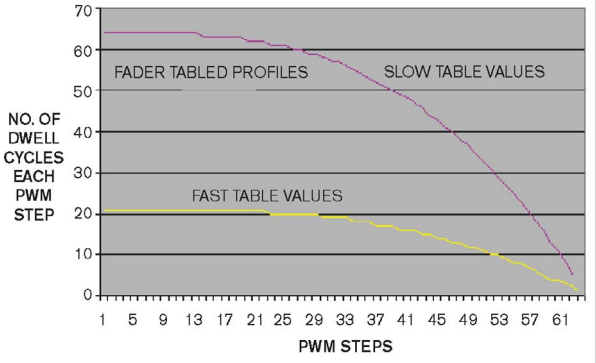

Figure 2 A table in the microcontroller code lets you run fast- or slow-fading profiles.

which you can download at the online version of this Design Idea at www.edn.com/091112dia). You can modify the code to build profiles of LEDs or incandescent lamps by applying a settable dwell time to each PWM step. The code contains two tables to set fast- and slow-fade characteristics. The fade values provide a cubed index that produces a 3-to-1 fade ratio (**Figure 2**). Using the final state of the output at Pin 3 of the 10F200, you access the tabled number of dwell cycles from the first table entry to the last for a high final state or from the last entry to the first to arrive at the final low state.

Fade-transition timing is user-selectable for either a 3- or a 9-second period. The circuit periodically samples both the fade rate and button or switch mode, allowing you to multiplex the design or use it in multiple configurations. The mode control is on Pin 5 of the controller, and the rate control is on Pin 4. The application exploits the controller's internal 4-MHz clock and the configurable pullup resistors on the monitored inputs. A prototype of the circuit uses a 10F20x in an eight-pin DIP, but the controller is also available in a smaller SOT-23 package. EDN

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RJK0394DPA			35	35	5.3	7.4	4.1	5.3	3.7	15.5	1.4
RJK0395DPA			30	30	7.6	10.6	5.9	7.7	2.6	11.0	2.2
RJK0396DPA			30	28	9.0	12.6	6.9	9.0	2.2	9	2.5
RJK0397DPA			30	25	10.4	14.6	7.8	10.1	1.9	7.4	2.5
RJK03B7DPA			30	30	7.7	10.7	6.0	7.8	2.6	11.0	1.0
RJK03B8DPA			30	28	9.3	12.9	7.0	9.3	2.2	9	1.2
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Outsourcing to China in question

Over the past two decades, a massive shift of manufacturing to China has occurred, especially for high-volume, low-mix electronics products. In recent years, however, a trend away from China has occurred, according to industry watchers and component distributors. Rising energy, transportation, and labor costs; IP (intellectual-property) issues; and counterfeit-IC problems are among the reasons they cite for the shift.

"We've seen a flurry of people jumping on the bandwagon to move from China," says Charlie Barnhart, co-founder and managing principal at Charlie Barnhart and Associates LLC (http://charliebarnhart.com), a company that studies outsourcing. "The trend started in 2006 as people started to see that [outsourcing to] Mexico was cheaper than [to] China."

Barnhart also notes that many OEMs are finding that the most efficient locations for outsourcing are near the end markets. "The cheapest and most effective outsourcing is building in the region for the region," he says. "Each region has a low-cost solution—Mexico for the Americas and Eastern Europe for Europe."

For a growing number of OEMs, proximity to the end customer has become the overriding concern in outsourcing. "I talk with customers about where they're going to outsource, and the number-one consideration is, 'Where is my customer?'" says Chuck Delph, senior vice president of sales at Avnet Electronics Marketing Americas, a division of Avnet Inc (www.avnet.com).

Even with the problems of manufacturing in China, some manufacturers have captured the benefits and swear by China's advantages. "Some OEMs are still pounding the table about the benefits of China," says Adam Pick, director and principal of EMS/OEM (electronics-manufacturing services/original-equipment manufacturing) at iSuppli Corp (www.isuppli.com). "They say, 'Yes, it was hard, but the result was astounding.'"

Meanwhile, manufacturing is once again warming up to North America. Companies including GlobalFoundries, Silicon Border, and Texas Instruments (www.globalfoundries.com, www.siliconborder.com, www.ti.com) have recently announced plans to open plants in the United States and Mexico.**—by Rob Spiegel**

GREEN UPDATE

MIIT PROPOSES CHINA ROHS CATALOG

China's Ministry of Industry and Information Technology (MIIT) in October issued the proposed Key Administrative Catalog for the Pollution Control of Electronic Information Products (Batch 1). More widely known as China ROHS (restriction of hazardous substances), the directive focuses on the same six substances as EU (European Union) ROHS: lead, mercury, cadmium, hexavalent chromium, PBB (polybrominated biphenyl), and PBDE (polybrominated-diphenyl ether). The catalog will apply to China ROHS Phase 2 restriction requirements. The restrictions are expected to come into force 10 months after the adoption of the legislation.

The catalog covers phones and printers, and MIIT will likely periodically update the list of products. Similar to EU ROHS restrictions, the catalog will allow some exemptions. The catalog requires testing, which manufacturers must conduct at specified labs in China. The catalog introduction follows China ROHS Phase 1 implementation in 2007, which required manufacturers to post labeling and recycling information on as many as 1800 electronic-information products.**—SD**

OUTLOOK

BLE SET FOR SURGE

ABI Research (www.abiresearch.com) expects manufacturers to ship some 2.5 billion BLE (Bluetooth low energy) chip sets in 2014, with most of those units being dual-mode ICs. The company reports that, by and large, separate groups of vendors, each dependent on the investment and commitment of the other, will produce dual- and single-mode ICs. Next year, single-mode ICs will account for less than 3% of BLE-chip-set shipments, according to the market-research company's data.

ABI Research estimates that manufacturers will ship more than 2.5 billion BLE chip sets in 2014 in a market that will grow at a 78% compound annual growth rate between 2009 and 2014. The company expects that less than one-third of those shipments will be for single-mode ICs. "BLE will enter the market in two stages—first with support for BLE embedded in mobile handsets and then with a second stage when BLE devices come to market," says Jonathan Collins, principal analyst at ABI Research.

Although low-power, short-range applications, such as sports and fitness equipment, will be the first devices to market, there is further potential for BLE health-monitoring applications. **—SD**

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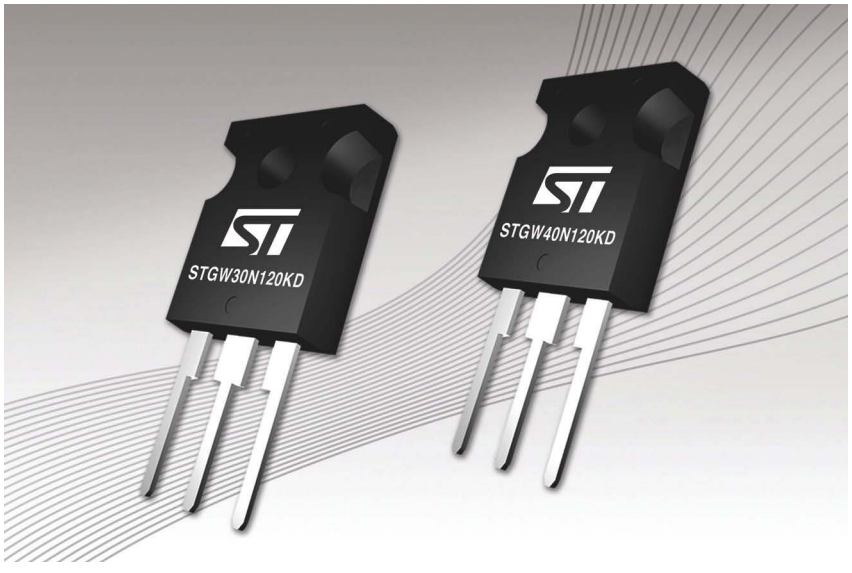

IGBTs use less energy than typical motor drives

The 30A STGW30N120KD and 40A STGW40N120KD IGBTs have low energy loss when conducting and switching. The devices come in TO-247 packages, which reduce component count by integrating ultrafast freewheeling diodes. Operating at 1200V, the transistors use high ac-line voltages, such as 440 or 480V, and can survive 10-µsec short circuits. The 30 and the 40A IGBTs cost $2.50 and $2.80 (5000), respectively.

STMicroelectronics, www.st.com

MOSFET comes in compact, high-current package

The TSON Advance MOSFET package reduces mount-area requirements by 64% in comparison with the 5×6-mm SOP-8 package. The TSON achieves a typical power dissipation of 1.9W. The series includes the 20V, N-channel TPCC8007; 30V, N-channel TPCC8008; and 30V, P-channel TPCC8102 and TPCC81036 devices. The TPCC8007 features a 20V drain-to-drain source voltage and a 27A drain current. Available in a 3.3×3.3×0.9-mm package, the TSON Advanced MOSFET series costs 30 cents each.

Toshiba America Electronic Components, www.toshiba.com/taec

Schottky-barrier diodes suit portable systems

The 30V NSR0xF30NXT5G and NSR0xL30NXT5G Schottky-barrier diodes feature solderable metal contacts under their packages, enabling designers to use the whole package area for active silicon. The NSR0xF30NXT5G has a 370-mV forward-voltage drop at 10 mA, and the NSR0xL30NXT5G provides a 1-µA reverse current at 10V reverse voltage. Options include a low forward voltage or low reverse current at 100- or 200-mA forward-current ratings. The diodes are available in 0.6×0.3×0.3-mm 0201DSN-2 chip-level packages, and prices start at 6 cents.

On Semiconductor, www.onsemi.com

30V MOSFET comes in Power 56 package

The 30V FDMS7650 MOSFET, targeting increased efficiency in server farms, functions as a load switch or an OR-ing FET. It provides a 0.99-mΩ maximum on-resistance, reducing conduction losses. Available in a Power 56 housing, the FDMS7650 MOSFET costs 95 cents (1000).

Fairchild Semiconductor, www.fairchildsemi.com

Industrial-grade MOSFET has low gate charge

The industrial-grade, 30V IRLB-8721PbF HEXFET power MOSFET provides low gate charge, suiting uninterruptible-power-supply inverters, low-voltage power tools, OR-ing applications, and Netcom and server power supplies. The MOSFET provides a 7.6- to 57-nC gate charge and a 4.5- to 2.6-mΩ on-resistance at 4.5V. The devices feature industrial-grade and moisture-sensitivity Level 1 qualifications. Available in a lead-free, ROHS-compliant TO-220 package, the IRLB8721PbF costs 22 cents (10,000).

International Rectifier, www.irf.com

productroundup

INTEGRATED CIRCUITS

Dual-channel RS-232 transceiver integrates fault protection

Providing pin compatibility with the vendor's MAX3223E, the ±70V fault-protected, dual-channel MAX13223E TS0232 transceiver targets applications requiring power and data transmission in one cable, such as automotive systems, telematics, base stations, utility meters, industrial equipment, point-of-sale terminals, and telecom equipment. Operating over 3 to 5.5V, the device provides an EIA/TIA-232 and V.28/V.24 communications interface. Functioning over a −40 to +85°C temperature range, the transceiver comes in a TSSOP-20 package and costs $2.70 (1000).

Maxim Integrated Products,
www.maxim-ic.com

Clock-generator IC suits broadcast-video applications

Aiming at professional-broadcast-video applications, the low-jitter Si5324 integrated-clock IC replaces typical multicomponent video-PLL devices with a clock IC. The device generates output frequencies of 2 kHz to 1.4 GHz from input frequencies of 2 kHz to 710 MHz. Additional features include a 5-psec-p-p jitter performance and an integrated, digitally programmable loop filter supporting loop bandwidths of 4 to 525 Hz. The IC is available in a 6×6-mm QFN-36 lead package, and prices range from $17.95 to $57.20 (1000), based on selected output-clock frequency ranges in A-, B-, C-, and D-speed grades.

Silicon Laboratories,
www.silabs.com

Rotary IC targets microcontroller-based automotive systems

Suiting automotive-safety applications, such as electronic-power-steering systems, the dual-die AS5215 magnetic rotary IC includes a programmable output-signal amplitude using sensitivity and gain settings. The IC provides selectable raw, inverted, or dc-referenced output-mode signals. The device features improved phase-matching and low sensitivity drift over a −40 to +125°C ambient-temperature range. Available in a TSSOP-14 package, the AS5215 magnetic rotary-encoder IC costs $6.40 (1000).

austriamicrosystems,
www.austriamicrosystems.com

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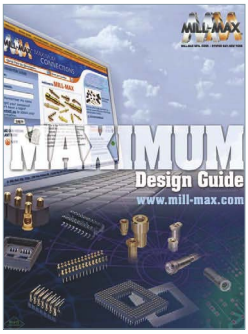

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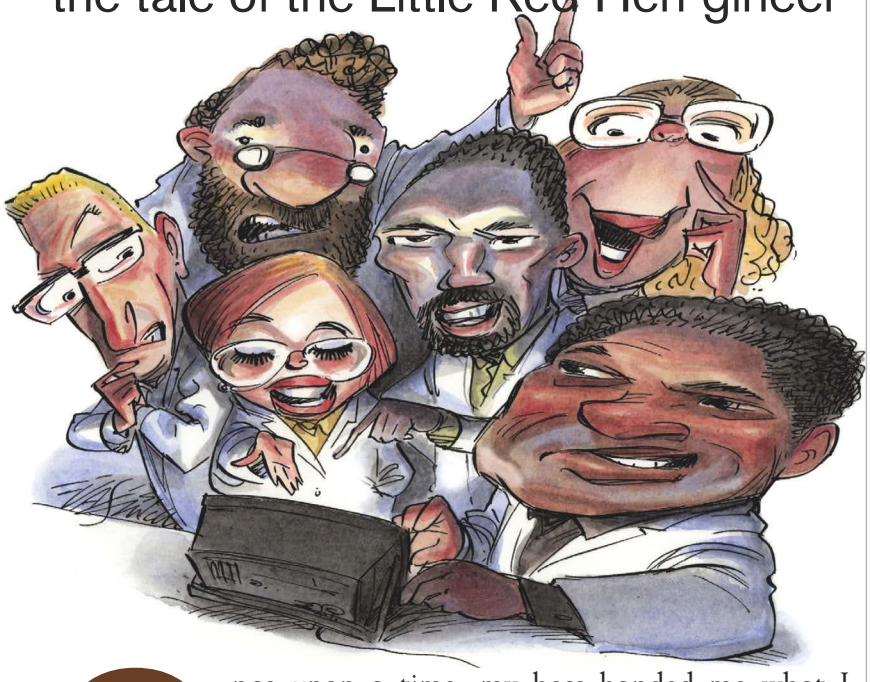
"Not I," said the rat: the tale of the Little Red Hen-gineer



Once upon a time, my boss handed me what I thought was a simple assignment: Build a receiver/demodulator for a multichannel PPM (pulse-position-modulated) data stream from a remote sensor. The sensor was a custom-built unit; I felt fortunate because the design was well-documented and we had spare units that I could play with. I soon found, however, that the sensor's designer had derived each channel's information pulses from the system's master clock, which was many times higher in frequency than the sensor's data signal. Because of this discrepancy, the information pulses were almost nonexistent, which caused problems with synchronization and decoding. It also made it next to impossible to see them on the oscilloscope, even with the brightness turned all the way up. So I asked my co-workers for help.

"You have too little energy in your signal," said my supervisor.

"Your pulses are too narrow," said my fellow lab-bench rat.

"Let me see the transmitter controller's source code," said the new hire. "That will tell me how to program the receiver."

I spent the next several days considering their comments until I realized they were either pointing out problems I had already seen or redesigning parts of the system that had nothing to do with the problems. So I went ahead with my design. When I asked for their opinions again, they responded:

"That preamp won't work. Use a comparator," said my supervisor.

"That filter will clip your pulses too much," said my fellow lab-bench rat.

"Where's the microcontroller?" asked the new hire. "How did you program this thing?"

I went back through my notes and diagrams, wondering whether I had missed something. I made changes, changed them back, tried different approaches, argued, explained, and then sat down and assembled a breadboard model. When they saw it, their comments were:

"It falls out of sync too easily," said my supervisor.

"Your error rate's too high," said my fellow lab-bench rat.

"You don't need all that stuff," said the new hire. "Here, I'll do a simulation. Then you can program a microcontroller to take care of your problems. This one's perfect for this job."

By now I was really exasperated, so I put the demodulator aside and worked on other projects. Then, late one night, the answer came to me: Change the modulation from pulse position to pulse width; it would add only a couple of flip-flops and some logic. In that way, I had an approximate square-wave output in the synchronous channel and longer stable voltage levels for the data channels. That combination meant there would be plenty of signal amplitude for synchronization and more setup time for the data registers. It also simplified my filter design.

When I showed my co-workers my now-working-correctly circuit, they had plenty of comments:

"So you took my advice," said my supervisor. "Be sure you spell all of our names correctly on your write-up. Oh, and be sure you log the time you spent on it this week."

"I told you it would work," said my fellow lab-bench rat. "Say, can you look at my data synchronizer? My problem's similar to yours."

"A microcontroller would've done it better," the new hire grumbled. "My stereo's doing something strange; would you mind taking a look at it?"

Well, I did learn something from this situation: It sometimes pays to shut off all the extra noise—um, information—and handle things your own way. I'm still having trouble, though, setting a proper noise threshold. EDN

Steve Lubs has been an engineer in a variety of roles at the Defense Department for 30 years.

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BY PANCH CHANDRASEKARAN

Get Up to Speed with Multi-Gigabit Serial Transceivers

Are you being asked to make your next-generation product design connect to a high-bandwidth network with an unfamiliar or a yet-to-be-defined protocol? Are you making the transition from parallel to serial I/O chip-to-chip communications? Or do you just need the highest-serial bandwidth, most reliable multi-gigabit transceivers the industry has to offer?

You are not alone. Serial connectivity is no longer just the design domain of communications engineers. Today, a growing number of designers in the consumer, automotive, industrial control, broadcast equipment, aerospace and defense markets are being tasked with developing products that employ multi-gigabit serial transceiver technology to communicate with next-generation, high-demanding, high-speed networks.

Today's quest for more bandwidth and better efficiency means that many designers like you must quickly get up to speed with the analog nuances of multi-gigabit serial transceivers. Luckily, Xilinx® has engineered its Targeted Design Platforms to help you.

Over the last two decades, the world's top telecommunications companies have relied upon Xilinx FPGAs' mix of logic functionality, high-speed memory, parallel connectivity, and serial I/O capabilities to create every generation of modern communications equipment.

With many years of experience serving the communication markets, Xilinx is able to help designers in a broad set of markets to quickly master gigabit serial transceiver technology and leverage it to create innovative products.

		MAINSTREAM	HIGH-END	ULTRA HIGH-END
	LINE RATES	▪ Up to 3.2Gpbs	▪ Up to 6.5Gpbs	▪ Beyond 11Gpbs
	FOCUS	▪ Simplicity, ease of design, and results	▪ Increased capabilities and performance	▪ Achieving breakthrough bandwdith
MARKET SEGMENTS	Wired	▪ Low-cost, efficient protocol bridging	▪ Advanced protocol mapping, performance optimized backplanes	▪ Cutting edge protocol support, advance processing capabilities
	Wireless	▪ Low-cost, Femto/ Picocell deployment	▪ Cost/Power efficient, mainstream deployment	
	Video Broadcast	▪ Efficient processing and routing capabilities	▪ Accelerated encoding and processing	▪ High-data aggregation/ routing, advanced processing capabilities
	Consumer	▪ Cost-effective integration, simplified serial interfaces		
	Automotive	▪ Low-power, cost-optimized, and flexible serial IO connectivity		
		SPARTAN LXT FPGAs	VIRTEX LXT FPGAs	VIRTEX HXT FPGAs

In 2009, Xilinx introduced both of its next-generation FPGA families — the high performance Virtex®-6 family and low-cost Spartan®-6 family providing Xilinx customers access to a full line of serial transceiver-rich FPGAs that can easily maintain line rates from up to 3.2Gbps in the Spartan-6 family, to up to 6.5Gbps in its Virtex-6 LXT devices, all the way beyond 11Gbps in the Virtex-6 HXT devices.

What's more, Xilinx announced this full range of serial connectivity-enabled FPGAs as the foundation of its new Targeted Design Platform strategy—combining the full line of transceiver-rich FPGAs with world-class tools, validated IP, reference designs, training, and support all delivered in domain and market specific kits. The Targeted Design Platforms allow customers to get their products to market faster than ever before.

With the ISE® Design Suite, customers can now get started on their designs targeting Virtex-6 HXT devices, as well as enhanced support for Spartan-6 LXT and Virtex-6 LXT and Virtex-6 SXT devices. Over the next several months, Xilinx will deliver a number of connectivity enabled design kits targeting wired, wireless broadcast video, packet processing, and traffic management application using either Virtex-6 devices for high performance, or Spartan-6 devices for low cost.

To learn more, visit the Connectivity Page at www.xilinx.com/connectivity where you'll find documentation, videos, links to software and IP downloads, and much more for helping you get up to speed no matter which fast lane you're on.

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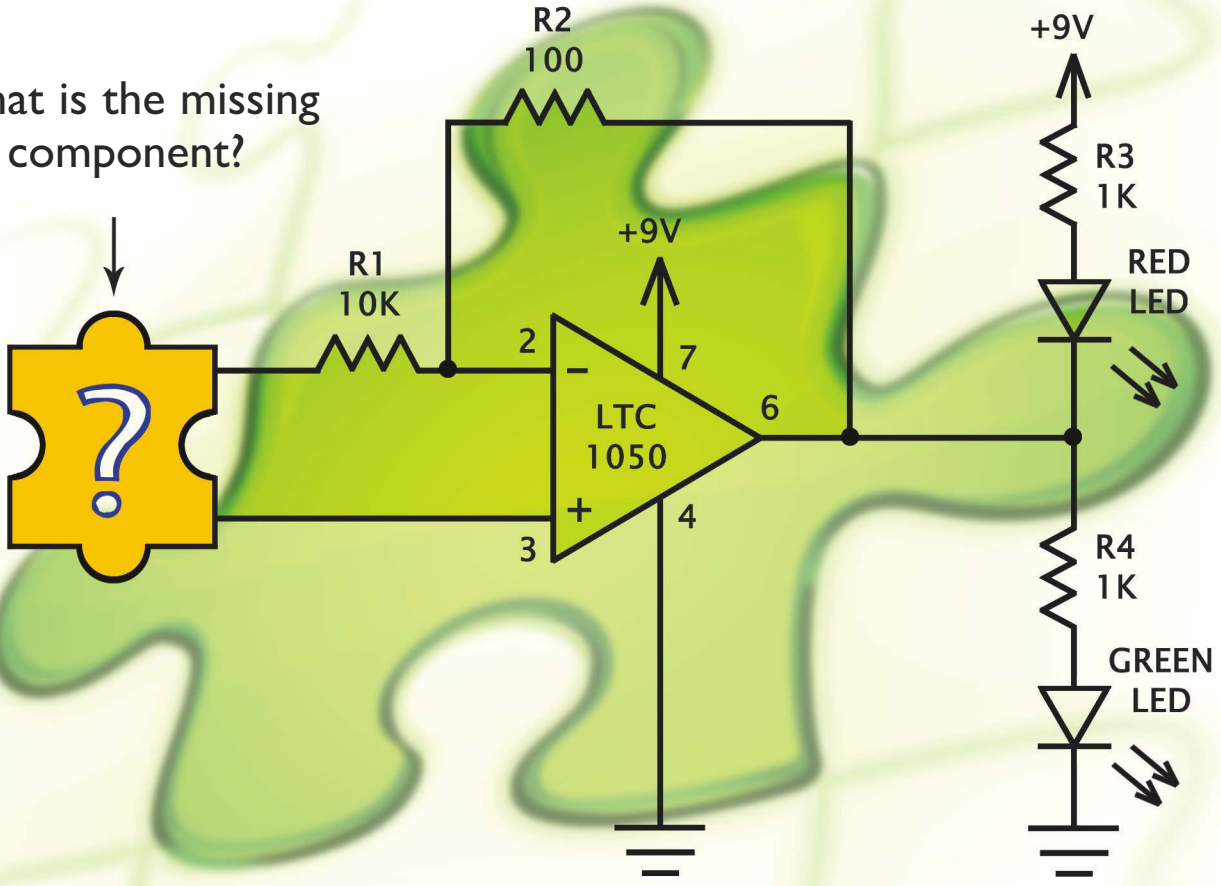
Are you up for a challenge?

What is the missing component?



Industry guru Forrest M. Mims III has created a stumper. Video game designer Bob Wheels needed an inexpensive, counter-clockwise rotation detector for a radio-controlled car that could withstand the busy hands of a teenaged game player and endure lots of punishment. Can you figure out what's missing? Go to www.Jameco.com/unfold to see if you are correct and while you are there, sign-up for our free full color catalog.

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